Pontificia Universidad Javeriana

Master Thesis Work

DC/DC High Voltage Multilevel Converter in Double Ladder Topology (Convertidor multinivel DC-DC de alto voltaje en topología escalera doble)

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January 17, 2012

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Chapter 1

Introduction

Classical switched power converters have some limitations in high voltage applications. They commonly require switching and passive energy storage components with operating voltages higher than the output voltage [1],[2]. With the increase of high voltage applications (several kilovolts), these converters, such as boost and buck, need high voltage and fast switching components, which are not fabricated with current technologies.

At the beginning of the 1990s, a new breed of power converters, called multilevel converters, appeared; these converters solved the problem of the high voltage on classical converters using a series connection of several basic cells [3], [4], [5], [6]. This technique allows the converter to manage high voltage using low voltage components. Multilevel converters have shown a good performance in high power applications [7], [8] for DC/DC [9], [10], [11] and DC/AC [12], [13], [14] conversion.

Within the multilevel topologies, there are some that use only capacitive storage elements such as Flying Capacitors and Ladder. Despite this type of converters, called switched capacitors converters, are widely used nowadays [15], [16], [17], due to its principle of functionality, they produce undesirable losses due to the capacitors charge process [18], [19]. Moreover, conduction and switching losses in the semiconductor devices and losses in the ESR of the capacitors occur because of the current spikes when two capacitors are interconnected [20], [21], [22], [23]. In [24], these current spikes are reduced using resonant techniques adding a small inductance in series with the capacitors, minimizing also the switching losses. Nevertheless, at high frequencies these inductors contribute to the converter losses [21].

Average models are widely used to obtain equivalent linear models of hybrid and non linear systems [25]. This eases the design of a control law allowing to use classical control design techniques [26, 27]. One of the possible applications for the average model is to find equilibrium points and admissible references in switched systems when the switching devices are assumed to be ideal [28].

The averaging technique is commonly used in power electronics (switching power supplies). It allows to remove the nonlinearities of the switching devices and obtain equivalent linearized models [29, 1, 30, 31, 32, 33, 34, 35]. Indeed, classical average models work under the assumption of slow state space dynamics compared to the period of one switching cycle. Although the classical technique

is simple, the assumptions of slow switching are not always fulfilled, leading to inaccurate models. In [36] several modeling techniques, such as Fourier series [37] and discrete time models [38] are reviewed. Also in [39] and [40] some drawbacks of the classical average model are discussed and alternative methods are mentioned. A modeling technique using series expansion, explained in more detail in [41, 42], corrects the error of the classical average model, nevertheless, it requires the assumption of a triangle ripple function in order to correctly estimate the average; this technique is also applied to a current control power converter in [43].

This document is organized as follows

Chapter 2

In this chapter three DC/DC ladder multilevel converters are compared. The first one is the classical ladder topology and the two other topologies presented are based on the classical one. A mathematical calculation of the output resistance and the gain of the converter as a function of the number of levels is carried out for the three topologies in order to estimate the voltage drop due to the output current. These calculations are validated with simulations and experimental results. Finally, the behavior of the three topologies is compared through experimental tests. Results show higher performance for the presented converters compared to the classical ladder.

Papers derived from this chapter: [44], [45], [46]

Chapter 3

In this chapter, a new technique of continuous modeling for switched systems represented as piecewise LTI systems over the state space variables is proposed. A procedure to calculate the Root Mean Square (RMS) value based on this technique is also enounced. In order to validate these models, a numerical example with a DC/DC power converter is used. The calculations of the state space matrices using the proposed model are performed and compared with the classical average model, and the time response is contrasted with simulations demonstrating its effectiveness. A linearized model of the proposed continuous model is obtained numerically due to its analytical complexity, and the frequency response for both models is also analyzed. The calculation of the RMS is validated with simulations.

Paper derived from this chapter: [47]

Chapter 4

In this chapter, different control methods for a classical ladder multilevel converter (CLT) (three levels) are evaluated. An analysis of the classical average model allows to chose an operation point. With the set of operation points, an uncertain model of the converter is constructed. Moreover, perturbation variables and performance masks are also defined. All this information is used to design an H_∞ "mixed sensitivity" and μ (DK) control laws for the uncertain case. The performance and robustness of the different controllers are compared through simulation with a classical PI control law.

Paper derived from this chapter: [48]

Chapter 5

The ladder multilevel converter uses switched capacitors in order to transfer energy between its input and its output. These types of converters have fast dynamics on each switching state compared to the switching frequency which produces model inaccuracies when the classical averaging modeling technique is applied. In this chapter two ladder multilevel converters (classical ladder topology (CLT) and double ladder topology (DLT)) are analyzed using a new averaging modeling technique. The CLT is analyzed using the classical and the new technique and the results are compared in order to illustrate the need of the procedure. Finally, a DLT converter of eight cells is analyzed and optimized for a glow discharge applications and some efficiency results are validated experimentally.

Paper derived from this chapter: [49]

Chapter 6

An accurate modeling technique is important in order to design a model-based control law. For switched system the classical state space averaging is a widely used modeling technique. However, this technique works under the assumption of slow dynamics of the state space variables. For certain power converters, such as switched capacitor converters, this assumption is not satisfied. In this chapter, comparisons of stability of robust control laws designed with the classical average are carried out in order to illustrate the need of a more accurate modeling technique. A ladder multilevel converter is modeled and analyzed using a new modeling technique for switched systems and its effectiveness is validated with experimental measurements. A robust control law is designed for a glow discharge application and its performance is tested experimentally.

Chapter 2

Analysis and Comparison of Three Topologies of the Ladder Multilevel DC/DC Converter

2.1 Introduction

The equivalent circuit of a switched capacitor converter in steady state is illustrated in Fig. 2.1. This equivalent circuit consists of a DC/DC transformer with turns ratio N and an equivalent output resistance R_{out} which represents all the losses and the output voltage dropout [9].

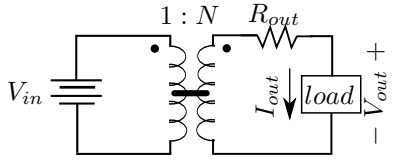


Figure 2.1: Equivalent model of a switched capacitor converter

This chapter analyzes the classical ladder multilevel topology and two variations. A general mathematic expression of R_{out} for the three topologies as a function of the number of cells is derived. In [23], the calculation of R_{out} is based on a state space model, this requires the re-computation of the matrices when a new cell is added or removed. The method proposed in this chapter allows the calculation of R_{out} as a function of the number of cells and without the computation of the state space matrices. The analysis proposed is validated through simulation and with experimental measurements using a prototype circuit. Finally it is demonstrated which topology produces less output resistance.

2.2 Classical ladder topology (CLT)

The classical ladder topology, shown in Fig. 2.2, is a simplified form of the flying capacitors topology. Both topologies (Classical ladder and Flying capacitors) are compared in [50]. The simplicity of the ladder topology is demonstrated since it requires less control signals an less switching and capacitive components [51]. As in [44], the converters studied in this work are analyzed as voltage elevators. However, since these converters are bidirectional [52], the analysis can be extended to step-down applications.

This topology requires only two control signals, HC_1 and its complementary HC_2. These control signals have a constant duty cycle d equal to 50%, leading to an ideal output voltage with N_c cells of

$$V_{out} = (N_c + 1)V_{in} \tag{2.1}$$

and the number of necessary capacitors N_{Cap} and switches N_S, as follows

$$\begin{aligned} N_{Cap} &= 2N_c \\ N_S &= 2N_c + 2 \end{aligned} \tag{2.2}$$

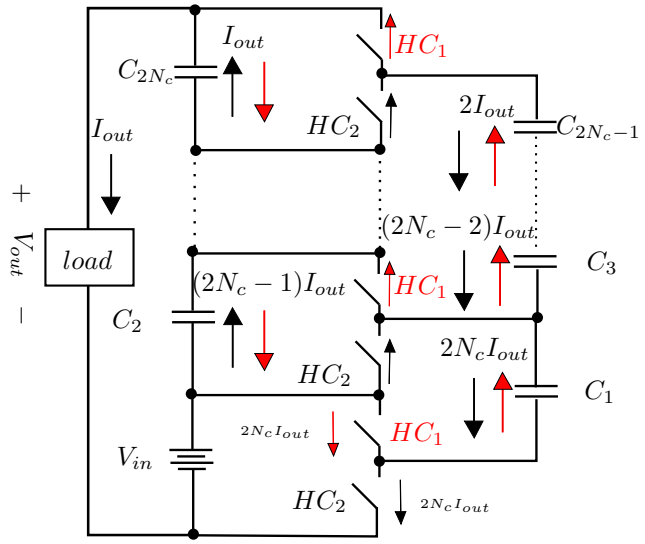


Figure 2.2: DC/DC voltage multilevel elevator in CLT with N_c cells. HC_1 denotes the half-cycle 1 and HC_2 the half-cycle 2. Average currents are shown during each half-cycle. The current through the switches is $2I_{out}$ except for those at the bottom cell.

The analysis of this topology is performed over its basic cell, shown in Fig. 2.3, without loss of generality

2.2.1 Basic Cell of the ladder topology

The basic cell of the ladder topology in Fig. 2.3 consists of two capacitive elements (C_1 and C_2) and four switching components (SW_1, SW_2, SW_3 and

SW_4). When SW_1 and SW_3 are ON, the input voltage source V_{in} charges the capacitor C_1. In the other half cycle, with SW_2 and SW_4 ON, the capacitor C_1 charges the capacitor C_2 leading, in an ideal case, to $V_{out} = 2V_{in}$

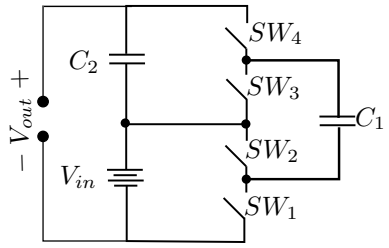


Figure 2.3: Basic cell of the ladder topology

The connection between capacitors, illustrated in Fig. 2.4, are affected by the ON resistance of the switches and the ESR of each capacitor, producing voltage drops. Furthermore, the time constant of the equivalent circuit (τ), which depends of the capacitance and resistance values, affects the current waveform on the capacitors: a large τ produces a square waveform, and a small τ produces an exponential waveform. These waveforms are illustrated in Fig. 2.5.

It is important to mention that when the equivalent τ is small compared with the switching period, the dynamic models of [31] can not produce an accurate model, because the conditions in [53] are not satisfied. However, alternative methods such as discrete time modeling can be used [54].

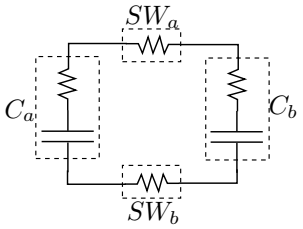


Figure 2.4: Connection between capacitors on a half-cycle

In steady state, the charge in the capacitor must be balanced, thus the average current in one switching period must be 0. In Fig. 2.5 both waveforms have the same average on each half cycle and 0 in the whole switching period, The exponential waveform has clearly higher spikes and therefore, a higher RMS value.

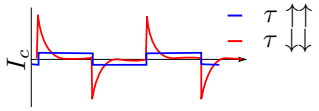


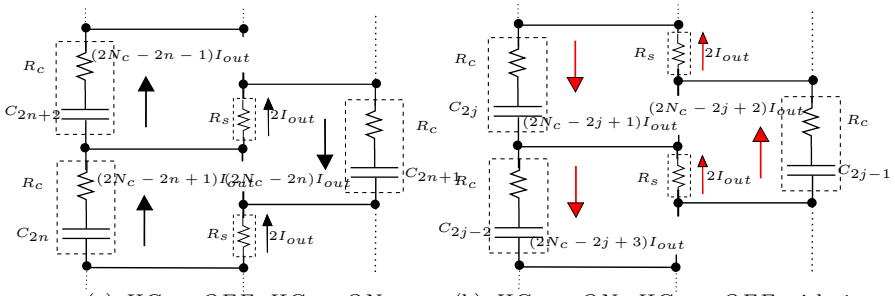
Figure 2.5: Current waveform for different τ values

This basic cell is the same for all the structures studied in this chapter.

2.2.2 Calculation of N and R_{out} for N_c cells

In order to evaluate the voltage drop due to the load current, it is necessary to calculate the output resistance R_{out} and obtain an expression which allows to scale the converter for design purposes. A mathematical analysis under the assumption of square current waveforms in the capacitors is performed in this section, considering two possible states.

For the following procedures R_c represents the ESR of the capacitors and R_s represents the ON resistance of the switches. The generalized connection between capacitors is as shown in Fig. 2.6.



(a) $HC_1 = OFF$, $HC_2 = ON$ (b) $HC_1 = ON$, $HC_2 = OFF$ with $j = n + 1$

Figure 2.6: Generalized connection between capacitors on each half-cycle

State 1 ($HC_1 = OFF$ and $HC_2 = ON$)

It is necessary to calculate the voltage of the capacitor C_1 in a different way than the voltage of the other capacitors since the current through the switches of the first cell is different compared to other cells, as seen in Fig. 2.2 (Note that the current of the switches connected to V_{in} is the same as for C_1; for all the other cases, is the current difference of the capacitors connected to the switch, i.e. $2I_{out}$). Therefore, this voltage is expressed as follows

$$V_{C_1} = V_{in} - 2I_{out}(N_c R_c + R_s(N_c + 1)) \tag{2.3}$$

where N_c is the number of cells in the converter. In general, for this half-cycle the connection between capacitors is as shown in Fig. 2.6(a). Therefore, the voltage of the capacitor C_{2n+1} can be expressed in terms of voltage of the capacitor C_{2n} as follows:

$$V_{C_{2n+1}} = V_{C_{2n}} - I_{out}(4N_c + 1 - 4n)R_c \tag{2.4}$$

where $n \in [1, N_c - 1]$. The output voltage V_{out} during this half cycle is the sum of the voltages of the capacitors with even subindex (C_2, C_4, ..., C_{2N_c}) plus V_{in} (see Fig. 2.2). Since each capacitor has an internal ESR, it is necessary to include its voltage drop. Therefore V_{out} can be expressed as

$$\begin{aligned} V_{out_1} =& V_{in} + \left[\sum_{n=1}^{N_c-1} (V_{C_{2n}} - (2N_c + 1 - 2n)I_{out}R_c)\right] \\ &+ V_{C_{2N_c}} - I_{out}R_c \end{aligned} \tag{2.5}$$

Note that the voltage drop in all the R_s resistances is cancelled, except at the bottom cell (2.3).

State 2 ($HC_1 = ON$ and $HC_2 = OFF$)

Again, it is necessary to calculate the voltage of the capacitor C_2 differently. This voltage can be expressed in terms of V_{C_1} as follows

$$V_{C_2} = V_{C_1} - I_{out}(2R_s(N_c + 1) + R_c(4N_c - 1)) \tag{2.6}$$

for this state the connection between capacitors is as shown in Fig. 2.6(b). Therefore, the voltage of the capacitor $V_{C_{2j}}$ can be expressed recursively as

$$V_{C_{2j}} = V_{C_{2j-1}} - I_{out}R_c(4N_c + 3 - 4j) \tag{2.7}$$

with $j = n + 1$. The output voltage, as in the previous case, can be expressed during this half cycle as

$$\begin{aligned} V_{out_2} =& V_{in} + V_{C_2} + (2N_c - 1)I_{out}R_c \\ &+ \left[\sum_{j=2}^{N_c} \left(V_{C_{2j}} + (2N_c - 1 - 2j)I_{out}R_c\right)\right] \end{aligned} \tag{2.8}$$

As in state 1, voltage drop in R_s resistances is only seen at the bottom cell (2.6).

Output Average Voltage

Since the duty cycle is constant and equal to 50%, the average output voltage $\overline{V_{out}}$ of the two previous cases is

$$\overline{V_{out}} = \frac{V_{out_1} + V_{out_2}}{2} = V_{in} + \sum_{m=1}^{N_c} V_{C_{2m}} \tag{2.9}$$

Note that the resistive drop is canceled. From (2.4) and (2.7) it can be obtained in terms of n

$$V_{C_{2n+2}} = V_{C_{2n}} - 4I_{out}R_c(2N_c - 2n) \tag{2.10}$$

The initial conditions for this difference equation are obtained from (2.3) and (2.6), where

$$V_{C_2} = V_{in} - I_{out}R_c(6N_c - 1) - 4I_{out}R_s(N_c + 1) \tag{2.11}$$

Solving the difference equation in (2.10), the voltage on the capacitors is

$$\begin{aligned} V_{C_{2m}} =& V_{in} - 4I_{out}R_s(N_c + 1) \\ &- I_{out}R_c(2N_c(4m - 1) - 4m^2 + 4m - 1) \end{aligned} \tag{2.12}$$

with $m \in [1, N_c]$. Using (2.9), $\overline{V_{out}}$ can be calculated, resulting in

$$\begin{aligned} \overline{V_{out}} =& V_{in}\underbrace{(N_c + 1)}_{N} \\ &- I_{out}\underbrace{\left[4N_cR_s(N_c + 1) + N_cR_c\frac{8N_c^2 + 6N_c + 1}{3}\right]}_{R_{out}} \end{aligned} \tag{2.13}$$

2.3 Symmetric Ladder Topology (SLT)

Fig. 2.7 shows the SLT. The functionality principle of this topology is the same as for CLT. It has two control signals, HC_1 and its complementary HC_2, with duty cycle d equal to 50%. The number of cells N_c must be even. A similar topology is used in [55] to maintain voltage balance in the capacitors of a diode-clamped converter. However, it is not analyzed as a voltage elevator considering parasitic resistances.

The main difference of this topology is how the current is distributed through the circuit (see Fig. 2.7). The current in the capacitors is up to $N_c I_{load}$ in contrast to $2N_c I_{load}$ of the CLT.

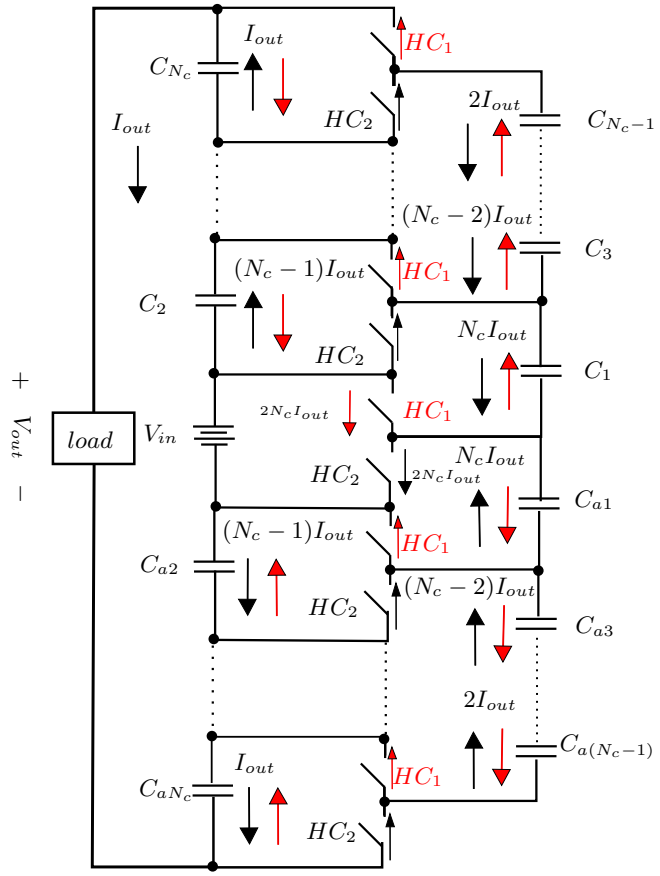


Figure 2.7: SLT as a DC/DC voltage multilevel elevator with N_c cells. HC_1 denotes the half-cycle 1 and HC_2 the half-cycle 2. Average currents are shown during each half cycle. The current through the switches is $2I_{out}$ except for those of the cell connected to the input voltage source V_{in}.

The number of necessary capacitors N_{Cap} and switches N_S for its implementation is

$$\begin{aligned} N_{Cap} &= 2N_c \\ N_S &= 2N_c + 2 \end{aligned} \tag{2.14}$$

One of the advantages of this topology is the interleaving between the upper-half part and the lower-half part of the circuit. Notice how, in the same half-cycle, the current in the capacitors C_n flows in the opposite direction of the current in the capacitors C_{an}. This implies that the converter output voltage and its input current have a smaller ripple than in CLT [56], [57], [58], as it is analyzed in the next subsection.

2.3.1 Calculation of N and R_{out} for N_c cells

In an analogous procedure as in Section 2.2.2, in this section, the output resistance R_{out} for the topology B is calculated under the assumption of square current waveforms.

State 1 ($HC_1 = OFF$ and $HC_2 = ON$)

The voltage of the capacitor C_1 for this topology is

$$V_{C_1} = V_{in} - I_{out}(N_c R_c + 2R_s(N_c + 1)) \tag{2.15}$$

Where N_c is the number of cells in the converter and must be even. The recursive expression of the capacitors voltage can be written as follows (see Fig. 2.6(a))

$$V_{C_{2n+1}} = V_{C_{2n}} - I_{out}(2N_c + 1 - 4n)R_c \tag{2.16}$$

where $n \in [1, N_c/2 - 1]$.

It is necessary to compute the voltage in the capacitors C_{an} to calculate the output voltage for this half-cycle. Thus, the voltage of the capacitor C_{a2} is

$$V_{C_{a2}} = V_{C_{a1}} - I_{out}(2R_s(N_c + 1) + R_c(2N_c - 1)) \tag{2.17}$$

and the recursive expression for the voltage of the capacitors C_{aj} is (see Fig. 2.6(b))

$$V_{C_{a(2j)}} = V_{C_{a(2j-1)}} - I_{out}R_c(2N_c + 3 - 4j) \tag{2.18}$$

with $j = n + 1$. Then the output voltage V_{out} for this half-cycle is

$$\begin{aligned} V_{out_1} =& V_{in} + \left[\sum_{n=1}^{N_c/2-1} (V_{C_{2n}} - (N_c + 1 - 2n)I_{out}R_c)\right] \\ &+ (V_{C_{N_c}} - I_{out}R_c) + (V_{C_{a2}} + (N_c - 1)I_{out}R_c) \\ &+ \left[\sum_{j=2}^{N_c/2} \left(V_{C_{a(2j)}} + (N_c - 1 - 2j)I_{out}R_c\right)\right] \end{aligned} \tag{2.19}$$

Note that in (2.19), the resistive voltage drop due to R_c is canceled, leading to

$$V_{out_1} = V_{in} + \sum_{n=1}^{N_c/2-1} (V_{C_{2n}}) + V_{C_{N_c}} + V_{C_{a2}} + \sum_{j=2}^{N_c/2} \left(V_{C_{a(2j)}}\right) \tag{2.20}$$

State 2 ($HC_1 = ON$ and $HC_2 = OFF$)

The voltage of the capacitor C_2 is

$$V_{C_2} = V_{C_1} - I_{out}(2R_s(N_c + 1) + R_c(2N_c - 1)) \tag{2.21}$$

The recursive expression for the voltage of the capacitors C_j, as in the previous cases, for this half cycle is

$$V_{C_{2j}} = V_{C_{2j-1}} - I_{out}R_c(2N_c + 3 - 4j) \tag{2.22}$$

with $j = n + 1$.

Again it is necessary to compute the voltage of the capacitors C_{an}. Then the voltage of the capacitor C_{a1} is

$$V_{C_{a1}} = V_{in} - I_{out}(N_cR_c + 2R_s(N_c + 1)) \tag{2.23}$$

and the recursive expression for the voltage of the capacitors C_{an} can be expressed as

$$V_{C_{a(2n+1)}} = V_{C_{a(2n)}} - I_{out}(2N_c + 1 - 4n)R_c \tag{2.24}$$

For this half-cycle, the output voltage can be written as follows

$$\begin{aligned} V_{out_2} =& V_{in} + \left[\sum_{n=1}^{N_c/2-1} \left(V_{C_{a(2n)}} + (N_c + 1 - 2n)I_{out}R_c\right)\right] \\ &+ (V_{C_{aN_c}} - I_{out}R_c) + (V_{C_2} + (N_c - 1)I_{out}R_c) \\ &+ \left[\sum_{j=2}^{N_c/2} \left(V_{C_{2j}} + (N_c - 1 - 2j)I_{out}R_c\right)\right] \end{aligned} \tag{2.25}$$

Again, the resistive voltage drop due to R_c is canceled, and the output voltage can be reduced to

$$V_{out_2} = V_{in} + \sum_{n=1}^{N_c/2-1} \left(V_{C_{a(2n)}}\right) + V_{C_{aN_c}} + V_{C_2} + \sum_{j=2}^{N_c/2} \left(V_{C_{2j}}\right) \tag{2.26}$$

Output Average Voltage

From (2.16), (2.22), (2.17) and (2.24) it can be obtained in terms of n

$$V_{C_{2n+2}} = V_{C_{a(2n+2)}} = V_{C_{2n}} - 4I_{out}R_c(N_c - 2n) \tag{2.27}$$

besides $V_{C_{a(2n)}} = V_{C_{2n}} = V_{C_{2m}}$ with $m \in [1, N_c/2]$. Therefore, the average output voltage $\overline{V_{out}}$ on the two half-cycles is

$$\overline{V_{out}} = \frac{V_{out_1} + V_{out_2}}{2} = V_{in} + 2\sum_{m=1}^{N_c/2} V_{C_{2m}} \tag{2.28}$$

Solving the difference equation in (2.27), the voltage of the capacitors is

$$\begin{aligned} V_{C_{2m}} =& V_{in} - 4I_{out}R_s(N_c + 1) \\ &- I_{out}R_c(N_c(4m - 1) - 4m^2 + 4m - 1) \end{aligned} \tag{2.29}$$

then, using (2.28), $\overline{V_{out}}$ can be expressed as follows

$$\begin{aligned}\overline{V_{out}} =& V_{in}\underbrace{(N_c+1)}_{N} \\ &- I_{out}\underbrace{\left[4N_cR_s(N_c+1)+N_cR_c\frac{2N_c^2+3N_c+1}{3}\right]}_{R_{out}}\end{aligned} \tag{2.30}$$

Table 2.1: Topology comparison

Topology	N_{Cap}	N_S	N	R_{out}	Ripple Cancelation
CLT	$2N_c$	$2N_c+2$	N_c+1	$4N_cR_s(N_c+1)+N_cR_c\frac{8N_c^2+6N_c+1}{3}$	No
SLT	$2N_c$	$2N_c+2$	N_c+1	$4N_cR_s(N_c+1)+N_cR_c\frac{2N_c^2+3N_c+1}{3}$	Yes
DLT	$2N_c$	$2N_c+4$	N_c+1	$2N_cR_s(N_c+2)+N_cR_c\frac{2N_c^2+3N_c+1}{3}$	Yes

2.4 Double Ladder Topology (DLT)

Fig. 2.8 shows the DLT, its principle of functionality is the same of the two previous topologies and, as for SLT, the number of cells N_c must be even

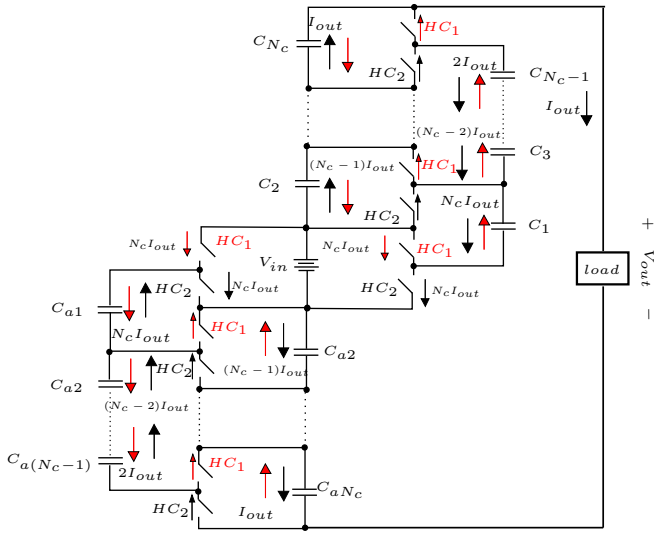


Figure 2.8: DLT of a DC/DC voltage multilevel elevator with N_c cells. HC_1 denotes the half-cycle 1 and HC_2 the half-cycle 2. Average currents are shown during each half-cycle. The current trough the switches is $2I_{out}$ except for those of the cell connected to the input voltage source V_{in}

For its implementation, the number of necessary capacitors N_{Cap} and switches N_S is

$$\begin{aligned}N_{Cap} &= 2N_c \\ N_S &= 2N_c+4\end{aligned} \tag{2.31}$$

This topology requires the same number of capacitors and two more switching devices in comparison with the two previous topologies. This topology has the same interleaving properties as SLT if the control signals are distributed as shown in Fig. 2.8, producing a small output voltage ripple and small input current ripple.

2.4.1 Calculation of N and R_{out} for N_c cells

The calculation of N and R_{out} for this topology is the same as for SLT. The difference between this topology and SLT is how the first capacitors are charged, therefore, these voltages (V_{C_1}, V_{C_2}, $V_{C_{a1}}$ and $V_{C_{a2}}$) need to be recalculated.

This section illustrates the calculation of the topology parameters using the results of SLT.

State 1 ($HC_1 = OFF$ and $HC_2 = ON$)

The voltage of the capacitor C_1 and C_{a2} is

$$V_{C_1} = V_{in} - I_{out}(N_c R_c + R_s(N_c + 2)) \tag{2.32}$$

$$V_{C_{a2}} = V_{C_{a1}} - I_{out}(R_c(2N_c + 1) + R_s(N_c + 2)) \tag{2.33}$$

The recursive expression of the voltage of the capacitors as well as the output voltage for this half cycle are the same as in (2.16), (2.18) and (2.20) respectively.

State 2 ($HC_1 = ON$ and $HC_2 = OFF$)

The voltage of the capacitor C_2 and C_{a1} is

$$V_{C_2} = V_{C_1} - I_{out}(R_s(N_c + 2) + R_c(2N_c + 1)) \tag{2.34}$$

$$V_{C_{a1}} = V_{in} - I_{out}(R_s(N_c + 2) + R_c N_c) \tag{2.35}$$

Again, the recursive expression and the output voltage for this half cycle are the same as in (2.22), (2.24) and (2.26) respectively.

Output Voltage Average

The difference equation for the capacitor voltages is the same as in (2.27). In contrast with the previous topology, the initial conditions for this equation are derived from (2.32), (2.33), (2.34) and (2.33) leading to the following result

$$\begin{aligned} V_{C_{2m}} =& V_{in} - 2I_{out}R_s(N_c + 2) \\ & - I_{out}R_c(N_c(4m - 1) - 4m^2 + 4m - 1) \end{aligned} \tag{2.36}$$

then, using (2.28), $\overline{V_{out}}$ is

$$\begin{aligned} \overline{V_{out}} =& V_{in}\underbrace{(N_c + 1)}_{N} \\ & - I_{out}\underbrace{\left[2N_c R_s(N_c + 2) + N_c R_c \frac{2N_c^2 + 3N_c + 1}{3}\right]}_{R_{out}} \end{aligned} \tag{2.37}$$

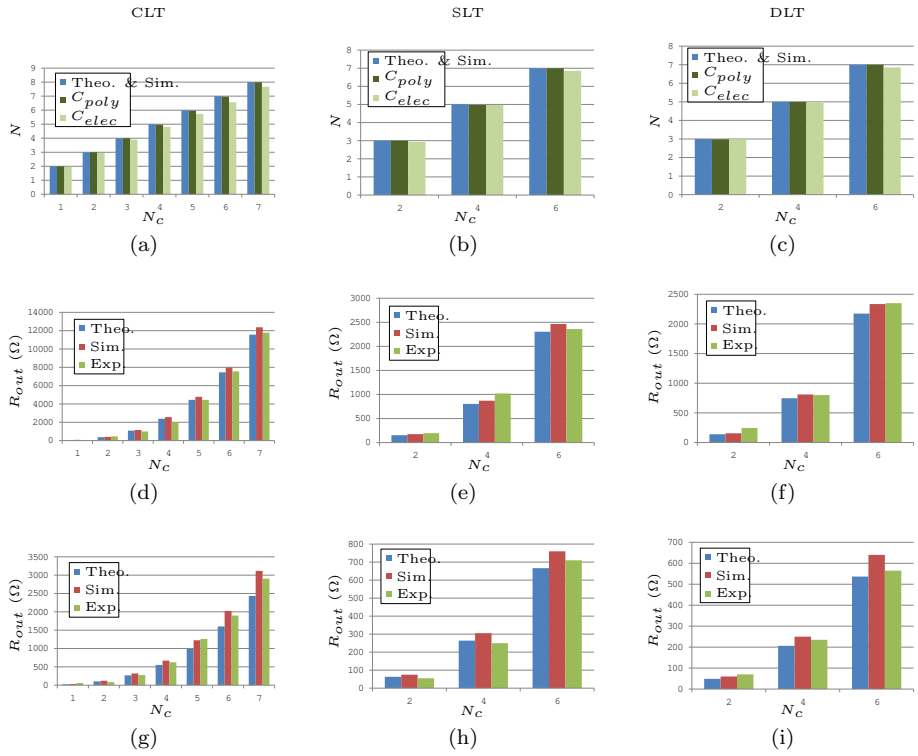


Figure 2.9: Comparison of theoretical, simulation and experimental results for CLT, SLT and DLT with capacitors C_{elec} and C_{poly} (a), (b), (c) Value of N without load for theoretical and simulation results, and experimental results for C_{poly} and C_{elec}; (d), (e), (f) Theoretical, simulation and experimental results of output resistance R_{out} for different values of N_c using the capacitor C_{elec}; (g), (h), (i) Theoretical, simulation and experimental results of output resistance R_{out} for different values of N_c using the capacitor C_{poly}

2.5 Topology comparison

Table 2.1 shows a comparison between the three topologies analyzed. Electrical and hardware characteristics are taken into account. For example, Table 2.2 shows a numerical comparison with $N_c = 6$, $R_c = 2\Omega$ and $R_s = 1.8\Omega$. Although DLT uses two more switching components, it can be observed that this topology has the lowest output resistance R_{out}, up to 3 times smaller than for CLT , producing less voltage drop.

Table 2.2: Topology comparison with $N_c = 6$, $Rc = 2\Omega$ and $R_s = 1.8\Omega$

Topology	N_{Cap}	N_S	N	R_{out}
CLT	12	14	7	1602Ω
SLT	12	14	7	666Ω
DLT	12	16	7	537Ω

2.6 Implementation and Experimental Results

2.6.1 Experimental set-up

In order to validate the theoretical analysis carried out for the three topologies in the previous sections, and to test the performance of the converter for a future application in a $3000V$, $100mA$ glow discharge; experimental measurements are taken. The measurements are made with an input voltage $V_{in} = 300V$ and an output current $I_{out} = 50mA$ and $I_{out} = 100mA$.

A P8NK100Z N-channel MOSFET is used as the switching component. This switch has a breakdown voltage of $1000V$ and an ON resistance $R_s = 1.8\Omega$.

For driving the *gate* control signals, four pulse transformers are employed, these transformers are built with $3000V$ isolation between each of its windings.

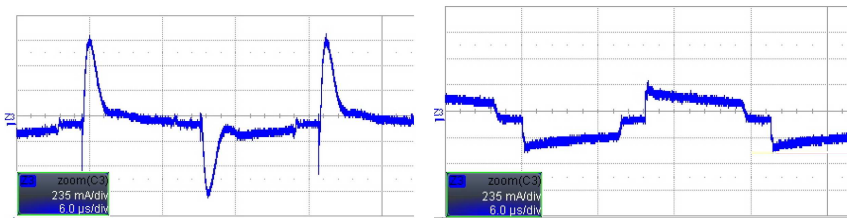
To evaluate the influence of the capacitor on the converter performance, two different capacitors are used as shown in Table 2.3.

2.6.2 Influence of the capacitor

The current waveform for each capacitor is shown in Fig. 2.10. It is observed that the electrolytic capacitor C_{elec} produces a square waveform due to its large ESR. On the other hand the polyester capacitor C_{poly} produces an exponential waveform due to its small ESR even with a larger capacitance value.

Table 2.3: Tested Capacitors

	Capacitance	ESR	Voltage	Material
C_{elec}	$1\mu F$	11Ω	$450V$	Aluminium (Electrolytic)
C_{poly}	$2,2\mu F$	2Ω	$450V$	Polyester



(a) C_{poly} (b) C_{elec}

Figure 2.10: Measured current waveform on the capacitors

2.6.3 Experimental results

The number of levels of the converter N_c are varied between 1 and 7. For SLT and DLT only even numbers are used. Figs. 2.9(a), (b) and (c) show the elevation ratio N with $I_{out} = 0mA$ for the three topologies.

Output current is set to $50mA$ and $100mA$ by a variable resistive load. The experimental output resistance of the converter R_{out} is calculated for both currents, and then, the average value is computed. Figs. 2.9(d), (e) and (f) show a comparison of theoretical, simulation and experimental results of the output resistance R_{out} using the capacitor C_{elec} for the three topologies. This procedure is also carried out using the capacitor C_{poly} (Figs. 2.9(g), (h) and (i)).

The experimental results in Fig. 2.9 show that the theoretical analysis is consistent with the experimental and simulation results. However, for the capacitor C_{poly}, a larger error is presented due to the exponential current waveform. Both current waveforms (exponential and square), have the same average in order to satisfy the charge balance on the capacitor. It can be seen that the exponential waveform has a higher AC component and therefore, a higher RMS. In the parasitic resistances, the losses are proportional to the RMS of the current, with higher losses for the exponential waveform. This can be observed for C_{elec} in Fig. 2.9(d), where the error between the theoretical and experimental results with $N_c = 7$ is less than 5%, whereas for C_{poly} the error is 17% (see Fig. 2.9(g)).

Despite the higher error of C_{poly}, for all the other topologies the output resistance is significatively less with this capacitor (see for SLT Figs. 2.9(e) and (h), for DLT Figs. 2.9(f) and (i)). For $N_c = 6$ the output resistance with C_{elec} is over 2000Ω for SLT and DLT. However, with C_{poly} is under 800Ω for the same two topologies.

For the capacitor C_{elec}, the value of the converter gain N is slightly reduced with the increase of the number of cells. This is mainly due to the switching losses. Since the current waveform is square, the switches are turned off with a higher current value than for an exponential waveform, producing higher switching losses. For SLT and DLT , this effect is reduced (see Figs. 2.9(a), (b) and (c)).

The results show that in general the capacitor C_{poly} produces less output resistance due to its lower ESR for the three topologies. Furthermore, with no load the capacitor C_{poly} does not produce voltage drop.

2.6.4 Topology comparison

Output resistance R_{out}

Fig. 2.11 shows a comparison of the experimental results for the three topologies with the capacitor C_{poly}. DLT shows, in general, less output resistance than the other two topologies. This is more noticeable for the capacitor C_{poly}, since in this case, a greater percentage of the value of R_{out} is due to the switches resistance R_s. For C_{elec}, DLT also shows less output resistance the the other two topologies (see Figs. 2.9(d), (e) and (f))

Output voltage ripple

Fig. 2.12 shows the measured voltage output ripple of CLT and DLT, as it is shown in the previous sections one of the advantages of DLT is the low voltage ripple. For SLT the voltage ripple is the same as for DLT, nevertheless SLT produces more voltage drop.

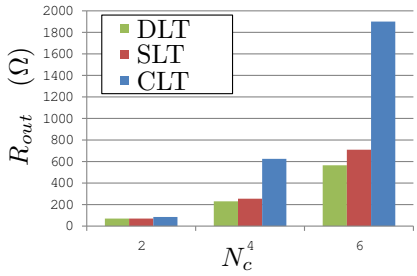


Figure 2.11: Comparison of experimental results for the three topologies using C_{poly}

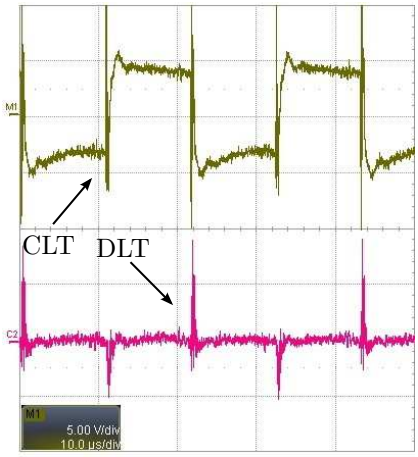


Figure 2.12: Output voltage ripple of CLT and DLT with $N_c = 4$, $V_{out} = 100V$ and $I_{out} = 100mA$

2.7 Conclusions

In this chapter three different DC/DC topologies of the ladder multilevel converter were analyzed. A mathematical calculation of the gain and the output resistance for each one of the three topologies were carried out. In order to validate the theoretical analysis a prototype circuit was implemented, and simulations were performed. It was shown that the mathematical expressions are consistent with the experimental and simulation results and they can be used as a design criterium.

It was demonstrated that the DLT, presented in this chapter reduces the output resistance compared with the other two topologies, leading to less losses. Also other advantages were mentioned, such as low input current ripple and low output voltage ripple. Nevertheless, since the outputs for SLT and DLT do not have the same reference as the input, it is difficult to measure the output variables, either current or voltage. In a high voltage application, the differential voltage between the outputs and the input reference can be several kilovolts, requiring high voltage isolation sensors.

The capacitors that produce less losses are those with small ESR and conse-

quently small time constant τ. In general the polyester capacitors have smaller ESR producing better results than electrolytic capacitors. However, a smaller time constant implies a higher current spike on the capacitors and switches which needs to be considered on the selection of these components.

As a future work, the dynamics of the converters will be studied, also control laws will be designed for the DLT converter in a glow discharge application [59].

Chapter 3

An Equivalent Continuous Model for Switched Systems

3.1 Introduction

Recently, new switched systems have been proposed for applications such as IC power converters and low distortion inverters [20, 8]. Some of these systems present fast dynamics, and the classical averaging technique cannot be used. Moreover, classical converters with a triangle ripple waveform, at low switching frequencies, present exponential ripple waveform, thus the technique in [41, 42] leads to inaccurate modeling. An alternative numerical technique that is able to model the system with an arbitrary ripple waveform is proposed in [60]. This chapter aims to analytically compute an equivalent continuous model for any switched system described by several LTI systems regardless of the speed of its dynamics. Equivalent state space matrices are obtained with analytical calculations conserving the nonlinearities related with the manipulable variables of the original system. In order to make it suitable in a general case, the method is presented for a class of switched systems with N modes. Analytical calculations for a special case of a boost power converter, which is described by two modes, are carried out.

The ripple waveform influences directly not only the average, but also the *RMS* value [61]. This value is directly related to the electric power dissipated by a resistive element in power electronics applications [22, 9, 1], which allows to estimate the power losses on transient and steady state. An *RMS* value calculation using the dynamics of the generalized equivalent continuous model, also enounced in this chapter, is proposed and validated.

The following notation and terminology will be used: All vectors are column vectors. If x is a vector, x^T is its transpose. $\langle x \rangle$ and $\|x\|_{RMS}$ are the average and *RMS* value of each element of vector x respectively. If A is a matrix, $\mathrm{diag}(A)$ represents a vector that has the diagonal elements of A, $\ker(A)$ is the null space of A. I is the identity matrix.

3.2 Classical Average Model and Problem Formulation

Let a switched system be described by N individual LTI subsystems

$$\dot{z} = \mathcal{A}_\sigma z + \mathcal{B}_\sigma u\,, \tag{3.1a}$$
$$y = \mathcal{C}_\sigma z + \mathcal{D}_\sigma u\,, \tag{3.1b}$$

where $\sigma \in [1, N] \subset \mathbb{Z}^+$, N is the number of subsystems (modes), $\mathcal{A}_\sigma \in \mathbb{R}^{\nu\times\nu}$, $\mathcal{B}_\sigma \in \mathbb{R}^{\nu\times\mu}$, $\mathcal{C}_\sigma \in \mathbb{R}^{d\times\nu}$, $D_\sigma \in \mathbb{R}^{d\times\mu}$; with $z \in \mathbb{R}^\nu$ the state vector and $y \in \mathbb{R}^d$ the output vector.

Assumption 1. *The system follows the mode sequence $\sigma = 1, \sigma = 2, \sigma = 3, \ldots, \sigma = N$, and the σ^{th} subsystem is ON for $d_\sigma T$ units of time (see Fig. 3.1).*

In the previous assumption T represents the duration of the whole sequence, also called the period of one switching cycle. d_σ is then the fraction of period in which the system stays in mode σ. Furthermore,

$$\sum_\sigma d_\sigma = 1 \tag{3.2}$$

must be satisfied.

The average of vector $\dot{z}$ can be written as

$$\langle \dot{z} \rangle = \frac{1}{T}\int_t^{t+T} \left(\sum_\sigma \mathcal{A}_\sigma z + \mathcal{B}_\sigma u \right) d\tau \tag{3.3}$$

and the average of the output vector y as

$$\langle y \rangle = \frac{1}{T}\int_t^{t+T} \left(\sum_\sigma \mathcal{C}_\sigma z + \mathcal{D}_\sigma u \right) d\tau\,. \tag{3.4}$$

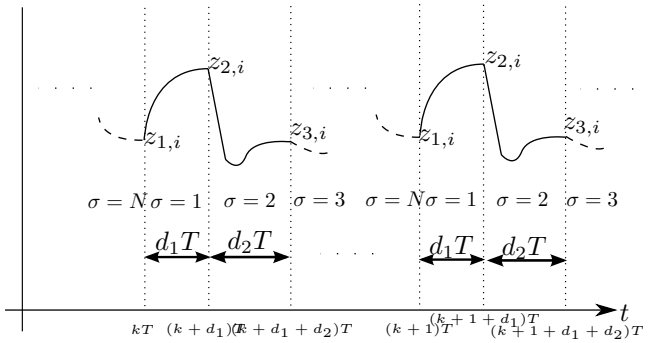


Figure 3.1: Switched system S, $k \in \mathbb{Z}^+$ and $z_{\sigma,i}$ is the initial condition of the state vector of subsystem σ

The classical average model, proposed in [53], approximates the dynamics of the system, described by the transition state matrix $e^{A_\sigma t}$, with the first

constant term of its series expansion $\langle e^{A_\sigma t} = I + A_\sigma t + \cdots \rangle$; this implies that the variations in the state vector through time must be slow compared with the value of T to verify the approximation. Besides, it is supposed that the input vector u has slow variations compared to the duration of one switching cycle. This approximation implies that (3.3) and (3.4) lead to the following results:

$$\langle \dot{z} \rangle = \sum_{\sigma} (\mathcal{A}_\sigma \langle z \rangle + \mathcal{B}_\sigma u) d_\sigma \,, \tag{3.5a}$$

$$\langle y \rangle = \sum_{\sigma} (\mathcal{C}_\sigma \langle x \rangle + \mathcal{D}_\sigma u) d_\sigma \,. \tag{3.5b}$$

Notice that d_σ is multiplying each vector field. This is an approximation of the real average model and it is a technique which is widely used in order to model power converters and obtain an equivalent linear system to easily design a control law [33, 1, 62, 63].

Suppose that each subsystem of the switched system (3.1) has dynamics as fast as (or even faster than) the duration of the sequence. Thus, the state transition matrix cannot be approximated as mentioned before and the model (3.5) will not represent the average behavior of the switched system (3.1). The problem that is addressed in this chapter is the following:

Problem 1. *Find an equivalent continuous model of the switched system* (3.1) *which describes its average dynamics regardless of the ratio between the variations in the state vector and the value of the duration of one switching cycle.*

3.3 General Equivalent Continuous Model

In order to consider the whole system dynamics, it is necessary to calculate the average of vector $\dot{x}$ considering the complete state transition matrix $e^{\mathcal{A}_\sigma t}$ for each subsystem. In contrast to the classical average model, for this analysis no approximation of this matrix is carried out. In the next subsections the mathematical procedure for the calculation of the general average model is explained.

3.3.1 Model

In order to simplify the analysis of the mathematical procedure, a new state space vector x be constructed as follows:

$$x = \begin{bmatrix} z^T & u^T \end{bmatrix}^T \,. \tag{3.6}$$

Therefore, the new system matrices are

$$A_\sigma = \begin{bmatrix} \mathcal{A}_\sigma & \mathcal{B}_\sigma \\ 0 & 0 \end{bmatrix}, \qquad C_\sigma = \begin{bmatrix} \mathcal{C}_\sigma & \mathcal{D}_\sigma \end{bmatrix}, \tag{3.7}$$

and the system is transformed into

$$\dot{x} = A_\sigma x \,, \tag{3.8a}$$

$$y = C_\sigma x \,, \tag{3.8b}$$

where $x \in \mathbb{R}^n$, $(n = \nu + \mu)$, A_σ and C_σ have suitable dimensions. Notice that the dimension of the state vector x is greater than that of the original vector z.

For each subsystem σ, the solution of the state equation is

$$x_\sigma(t) = \varphi_\sigma(t, x_{\sigma,i}) = \phi_\sigma(t) x_{\sigma,i} \tag{3.9}$$

where

$$\phi_\sigma(t) = e^{A_\sigma t}$$

and $x_{\sigma,i}$ is the initial condition of the state vector x for mode σ.

The multiplication of the ϕ_σ matrices is carried out by the operator Λ which is defined as

$$\Lambda(a,b) = \begin{cases} \prod_{j=1}^{a} \phi_{b-j}(d_{b-j}T)\,, & 1 \le a \le N \wedge 1 + a \le b \le N + a\,; \\ I\,, & \sim\,. \end{cases} \tag{3.10}$$

With the solution of the state equation for each subsystem, the initial condition of the state vector of subsystem $\sigma + 1$ can be expressed as a function of the initial condition of the state vector of subsystem σ as

$$x_{\sigma+1,i} = \varphi_\sigma(d_\sigma T, x_{\sigma,i})\,. \tag{3.11}$$

Moreover, the initial condition of the first subsystem $\sigma = 1$ can be expressed in terms of the initial condition of the last subsystem $\sigma = N$ as

$$x_{1,i} = \varphi_N(d_N T, x_{N,i})\,. \tag{3.12}$$

The equivalent continuous model, which is one of the main results presented in this chapter, follows.

Proposition 1. *Let the switched system be described by* (3.8)*. Then, an equivalent continuous model which describes its behavior in average is*

i) Dynamics of the state x

$$\langle \dot{x} \rangle = \langle A \rangle \langle x \rangle\,, \quad \langle A \rangle = \Gamma A_c \Gamma^{-1}\,, \tag{3.13}$$

where

$$A_c = \frac{1}{T} \ln(A_\delta)\,, \tag{3.14}$$

$$A_\delta = \Lambda(N, N+1)\,, \tag{3.15}$$

$$\Gamma = \sum_{j=1}^{N} \Omega_j \Lambda(j-1, j)\,, \tag{3.16}$$

and

$$\Omega_j = \frac{1}{T} \int_0^{d_j T} \phi_j(\tau) d\tau\,. \tag{3.17}$$

ii) Dynamics of the output y

$$\langle y\rangle = \langle C\rangle\langle x\rangle, \quad \langle C\rangle = \Gamma_C\Gamma^{-1}\,, \tag{3.18}$$

where

$$\Gamma_C = \sum_{j=1}^{N} C_j\Omega_j\Lambda(j-1,j)\,. \tag{3.19}$$

Proof. Part *i)* of Proposition 1 consists of the continuous model for the state x. Using (3.11) and (3.12), the initial condition of the subsystem $\sigma = 1$ in $t = (k+1)T$ can be expressed as a function of the initial condition of the same subsystem in $t = kT$, with $k \in \mathbb{Z}^+$ as

$$x_{1,i}((k+1)T) = A_\delta x_{1,i}(kT) \tag{3.20}$$

where A_δ is defined in (3.15). Notice that the matrix A_δ has the form

$$A_\delta = \begin{bmatrix} \mathcal{A}_\delta & \mathcal{B}_\delta \\ 0 & I \end{bmatrix}. \tag{3.21}$$

Matrices $\mathcal{A}_\delta$ and $\mathcal{B}_\delta$ are part of the state space model of the original vector z and its initial conditions $z_{1,i}$:

$$z_{1,i}((k+1)T) = \mathcal{A}_\delta x_{1,i}(kT) + \mathcal{B}_\delta u(kT)\,. \tag{3.22}$$

On the other hand, the mobile average of any subsystem can be expressed as

$$\frac{1}{T}\int_{t+\sum_{j=1}^{m-1} d_jT}^{t+\sum_{j=1}^{m-1} d_jT+\alpha} \varphi\left(\tau + t + \sum_{j=1}^{m-1} d_jT, x_{m_i}\right) d\tau = \frac{1}{T}\int_0^\alpha \varphi(\tau, x_{m_i})d\tau$$

Therefore, the average of the state vector in (3.9) is

$$\langle x\rangle = \sum_{j=1}^{N} \frac{1}{T}\int_0^{d_jT} x_j(t)\,dt\,, \tag{3.23}$$

which, using (3.9), can be written as

$$\langle x\rangle = \sum_{j=1}^{N} \frac{1}{T}\int_0^{d_jT} \varphi_j(t, x_{j,i})\,dt\,. \tag{3.24}$$

With (3.11) and (3.12), the initial conditions of subsystem $\sigma = j$, $x_{j,i}$, can be written as a function only of the initial conditions of subsystem $\sigma = 1$, $x_{1,i}$, using (3.10) as follows:

$$x_{j,i} = \Lambda(j-1,j)x_{1,i}\,. \tag{3.25}$$

Then (3.24) can be expressed in the form

$$\langle x\rangle = \Gamma x_{1,i}\,. \tag{3.26}$$

Now it is necessary to include the dynamics of the initial conditions of the model, and the state vector average on a continuous system. The continuous system can bee obtained with a classical transformation between a discrete and a continuous system as it is indicated in (3.14).

From (3.26),

$$\langle \dot{x} \rangle = \Gamma \dot{x}_{1,i} \,. \tag{3.27}$$

Finally, with (3.26) and (3.27), the dynamics of the general average model can be written as it is shown in (3.13).

Part *ii)* of the proof focuses on the dynamics of y. Using (3.7), the average of the output vector y can be written as

$$\langle y \rangle = \frac{1}{T} \int_t^{t+T} \left(\sum_\sigma C_\sigma x \right) d\tau. \tag{3.28}$$

This term can be expressed as a function of the initial conditions of the model $\sigma = 1$, $x_{1,i}$ and, analyzing as for the state vector x,

$$\langle y \rangle = \Gamma_C x_{1,i} \tag{3.29}$$

where Γ_C is given by (3.19).

With (3.26), the average of the output vector y can be expressed in terms of the average of the state vector as (3.18). □

Remark 1. *Ω_j can be computed analytically, or numerically in the case that matrix A is singular or badly scaled.*

Remark 2. *Matrix $\langle A \rangle$ has the form*

$$\langle A \rangle = \begin{bmatrix} \langle \mathcal{A} \rangle & \langle \mathcal{B} \rangle \\ 0 & 0 \end{bmatrix} \tag{3.30}$$

where matrices $\langle \mathcal{A} \rangle$ and $\langle \mathcal{B} \rangle$ are part of the state space model of the original vector z

$$\langle \dot{z} \rangle = \langle \mathcal{A} \rangle \langle z \rangle + \langle \mathcal{B} \rangle u \,. \tag{3.31}$$

Remark 3. *Matrix $\langle C \rangle$ has the form*

$$\langle C \rangle = \begin{bmatrix} \langle \mathcal{C} \rangle & \langle \mathcal{D} \rangle \end{bmatrix} \tag{3.32}$$

where matrices $\langle \mathcal{C} \rangle$ and $\langle \mathcal{D} \rangle$ are part of the state space model of the original vector z

$$\langle y \rangle = \langle \mathcal{C} \rangle \langle z \rangle + \langle \mathcal{D} \rangle u \,. \tag{3.33}$$

It is important to notice that if the switching frequency tends to infinity, the classical average model and the model in Proposition 1 yield the same results.

3.3.2 Linearization

In order to easily design the control laws, an input-output linearized model is always desired. Thus, it is necessary to eliminate the nonlinearities associated with the input variables. It can be observed that matrix $\langle A \rangle$ given in (3.13) can be written using operator Λ from (3.10) which is function of the state transition

matrix $\phi_\sigma(dT)$. Therefore, matrix $\langle A \rangle$ is a non linear function with respect to the input d_σ. Notice that the linearization process does not simplify the dynamics of the system in the operation point, this is the main difference with the assumption of the classical model that simplifies the state transition matrix to a constant term, simplifying its dynamics.

Let $d_\sigma = \bar{d}_\sigma + \tilde{d}_\sigma$, where $\bar{d}_\sigma$ produces an operation point $\langle \bar{x} \rangle$, i.e. $\langle \bar{x} \rangle \in \ker\left(\langle A \rangle|_{\bar{d}_\sigma}\right)$, and $\tilde{d}_\sigma$ is the increments. The linearized model can be written as follows

$$\begin{aligned} \langle \dot{\tilde{x}} \rangle &= \langle \tilde{A} \rangle \langle \tilde{x} \rangle + \langle \tilde{B}_{d_\sigma} \rangle \tilde{d}_\sigma \,, \\ \langle \tilde{y} \rangle &= \langle \tilde{C} \rangle \langle \tilde{x} \rangle + \langle \tilde{D}_{d_\sigma} \rangle \tilde{d}_\sigma \,, \end{aligned} \tag{3.34}$$

where

$$\langle \tilde{A} \rangle = \langle A \rangle|_{\bar{d}_\sigma}, \quad \langle \tilde{B}_{d_\sigma} \rangle = \left(\left. \frac{\partial \langle A \rangle}{\partial d_\sigma} \right|_{\bar{d}_\sigma} \langle \bar{x} \rangle \right),$$

$$\langle \tilde{C} \rangle = \langle C \rangle|_{\bar{d}_\sigma}, \quad \langle \tilde{D}_{d_\sigma} \rangle = \left(\left. \frac{\partial \langle C \rangle}{\partial d_\sigma} \right|_{\bar{d}_\sigma} \langle \bar{x} \rangle \right).$$

Remark 4. *Matrices $\langle \tilde{B}_{d_\sigma} \rangle$ and $\langle \tilde{D}_{d_\sigma} \rangle$ have the form*

$$\langle \tilde{B}_{d_\sigma} \rangle = \begin{bmatrix} \langle \tilde{\mathcal{B}}_{d_\sigma} \rangle \\ 0 \end{bmatrix}, \quad \langle \tilde{D}_{d_\sigma} \rangle = \begin{bmatrix} \langle \tilde{\mathcal{D}}_{d_\sigma} \rangle \\ 0 \end{bmatrix},$$

where matrices $\langle \tilde{\mathcal{D}}_{d_\sigma} \rangle$ and $\langle \tilde{\mathcal{B}}_{d_\sigma} \rangle$ are part of the state space model of the original vector z. Remember that matrices $\langle A \rangle$ and $\langle C \rangle$ have the form described in remark 2 and remark 3, respectively. Therefore, $\langle \tilde{A} \rangle$ and $\langle \tilde{C} \rangle$ have the same form.

Since an analytical linearization is mathematically complex, it is proposed to carry out a numerical calculation that approximates the derivatives as follows:

$$\left. \frac{\partial \langle A \rangle}{\partial d_\sigma} \right|_{\bar{d}_\sigma} \approx \frac{\langle A \rangle|_{\bar{d}_\sigma + \Delta_{d_\sigma}} - \langle A \rangle|_{\bar{d}_\sigma - \Delta_{d_\sigma}}}{2\Delta_{d_\sigma}}, \tag{3.35}$$

$$\left. \frac{\partial \langle C \rangle}{\partial d_\sigma} \right|_{\bar{d}_\sigma} \approx \frac{\langle C \rangle|_{\bar{d}_\sigma + \Delta_{d_\sigma}} - \langle C \rangle|_{\bar{d}_\sigma - \Delta_{d_\sigma}}}{2\Delta_{d_\sigma}}, \tag{3.36}$$

where Δ_{d_σ} is a small variation of d_σ and must be small enough in order to obtain a good approximation. This analysis can be extended to any other variable matrices $\langle A \rangle$ and $\langle C \rangle$ depend on.

3.4 *RMS* Value

See [47] in the attached papers.

3.5 Two sub models case example

In this section, results of the conventional average model and the equivalent continuous model are calculated for a typical case with only two sub models ($N = 2$). Also assuming $d_1 = d$ and $d_2 = 1 - d$.

Suppose a power converter in boost configuration as shown in Fig. 3.2. S_1 and S_2 represent switches; L and R_L an inductance an its series resistance; C a capacitor and R the load resistance.

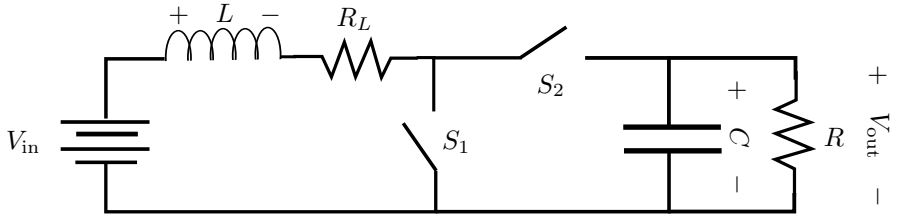


Figure 3.2: Boost power converter

The converter works at a constant switching frequency f. The switches S_1 and S_2 are complementary, and S_1 is turned-on during a time equal to d/f and its complementary, S_2, during $(1-d)/f$. The state space variables are the inductor current i_L and the capacitor voltage v_C. The input variable is V_{in}. Therefore the state space vector x and the input vector u are

$$z = [i_L \quad v_C]^T\,, \qquad\qquad u = V_{\text{in}}\,. \tag{3.37}$$

The output of the system is the load voltage V_{out} which is equal to v_C. Thus, the state space matrices of the systems for $\sigma = 1$ are

$$\begin{aligned} \mathcal{A}_1 &= \begin{bmatrix} -\frac{R_L}{L} & 0 \\ 0 & -\frac{1}{CR} \end{bmatrix}, & \mathcal{B}_1 &= \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix}, \\ \mathcal{C}_1 &= \begin{bmatrix} 0 & 1 \end{bmatrix}, & \mathcal{D}_1 &= 0\,; \end{aligned} \tag{3.38}$$

and for $\sigma = 2$

$$\begin{aligned} \mathcal{A}_2 &= \begin{bmatrix} -\frac{R_L}{L} & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{CR} \end{bmatrix}, & \mathcal{B}_2 &= \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix}, \\ \mathcal{C}_2 &= \begin{bmatrix} 0 & 1 \end{bmatrix}, & \mathcal{D}_2 &= 0\,. \end{aligned} \tag{3.39}$$

The numeric values of the parameters are $L = 0.1$ mH, $R_L = 5\ \Omega$, $C = 40\ \mu$F, $R = 100\ \Omega$, $f = 6$ kHz, and $d = 0.6$.

3.5.1 Classical average model

As shown in (3.5), the classical average model can be written as

$$\langle \dot{x} \rangle = (\mathcal{A}_1 d + \mathcal{A}_2(1-d))\langle x \rangle + (\mathcal{B}_1 d + \mathcal{B}_2(1-d))u\,, \tag{3.40a}$$

$$\langle y \rangle = (\mathcal{C}_1 d + \mathcal{C}_2(1-d))\langle x \rangle + (\mathcal{D}_1 d + \mathcal{D}_2(1-d))u\,. \tag{3.40b}$$

Then the state space matrices are

$$\begin{aligned} \langle \mathcal{A} \rangle &= \mathcal{A}_1 d + \mathcal{A}_2(1-d)\,, & \langle \mathcal{B} \rangle &= \mathcal{B}_1 d + \mathcal{B}_2(1-d)\,, \\ \langle \mathcal{C} \rangle &= \mathcal{C}_1 d + \mathcal{C}_2(1-d)\,, & \langle \mathcal{D} \rangle &= \mathcal{D}_1 d + \mathcal{D}_2(1-d)\,. \end{aligned} \tag{3.41}$$

Using the numerical values of the boost converter, the matrices can be written as follows

$$\begin{aligned} \langle \mathcal{A} \rangle &= \begin{bmatrix} -20 & -4 \\ 10 & -0.25 \end{bmatrix} \cdot 10^3 \,, & \langle \mathcal{B} \rangle &= \begin{bmatrix} 10 \\ 0 \end{bmatrix} \cdot 10^3 \,, \\ \langle \mathcal{C} \rangle &= \begin{bmatrix} 0 & 1 \end{bmatrix} \,, & \langle \mathcal{D} \rangle &= 0 \,. \end{aligned} \tag{3.42}$$

This model is valid only for $d = 0.6$.

3.5.2 General equivalent continuous model

Matrices A_δ, Γ, and Γ_C – from (3.15), (3.16), and (3.19) respectively – for a two sub models case are

$$A_\delta = \Lambda(2,3) = \phi_2((1-d)T)\phi_1(dT) \,, \tag{3.43}$$

$$\Gamma = \Omega_1 \Lambda(0,1) + \Omega_2 \Lambda(1,2) \,, \tag{3.44}$$

$$\Gamma_C = C_1 \Omega_1 \Lambda(0,1) + C_2 \Omega_2 \Lambda(1,2) \,, \tag{3.45}$$

where $\Lambda(0,1) = I, \Lambda(1,2) = \phi_1(dT)$. Using these, matrices $\langle A \rangle$ y $\langle C \rangle$ can be computed with (3.13) and (3.18). $\langle \mathcal{A} \rangle$ and $\langle \mathcal{B} \rangle$ can be decomposed using (3.30) and (3.32) respectively, leading to the following numerical results for the boost converter:

$$\begin{aligned} \langle \mathcal{A} \rangle &= \begin{bmatrix} -18.72 & -3.83 \\ 7.17 & -1.53 \end{bmatrix} \cdot 10^3 \,, & \langle \mathcal{B} \rangle &= \begin{bmatrix} 9.32 \\ 1.70 \end{bmatrix} \cdot 10^3 \,, \\ \langle \mathcal{C} \rangle &= \begin{bmatrix} 0 & 1 \end{bmatrix} \,, & \langle \mathcal{D} \rangle &= 0 \,. \end{aligned} \tag{3.46}$$

This model is valid only for $d = 0.6$. The results in (3.42) and (3.46) show a noticeable difference on the numerical values of the resulting state space matrices $\langle \mathcal{A} \rangle$ and $\langle \mathcal{B} \rangle$. However, the results for $\langle \mathcal{C} \rangle$ and $\langle \mathcal{D} \rangle$ are equal.

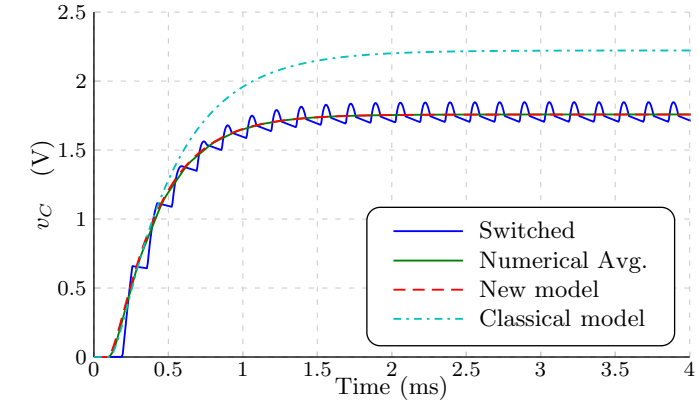
Fig. 3.3 shows the step response of the state space variables of the classical average model and the general equivalent continuous model compared with the simulated converter and the calculated average which was numerically computed in simulation. Clearly, the model proposed in this work is able to model the real converter dynamics with more accurate results than the classical average model. The classical average fails to model the DC gain of the converter for both variables, i_L and v_C. Some additional comparisons of the dynamics are performed in the next subsection.

3.5.3 Linearization

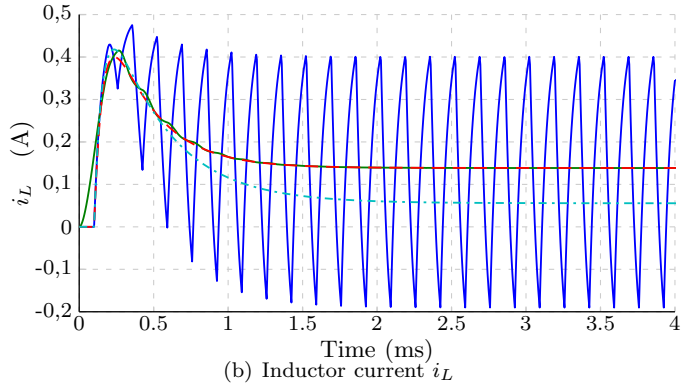
Since the system dynamics dependence on parameter d is not linear, a linearization is performed. Further information on the linearization process can be found in [1].

The new input vector for the linearized system is

$$\tilde{u} = \begin{bmatrix} \tilde{V}_{\text{in}} & \tilde{d} \end{bmatrix}^T \tag{3.47}$$



(a) Capacitor voltage v_C



(b) Inductor current i_L

Figure 3.3: Comparison of a unitary step response from V_{in} to V_{out}

where $V_{\text{in}} = \bar{V}_{\text{in}} + \tilde{V}_{\text{in}}$ and $d = 0.6 + \tilde{d}$. The linearized model is valid only for small values of $\tilde{d}$ and $\tilde{V}_{\text{in}}$, i.e $\tilde{d} \ll 0.6$ and $\tilde{V}_{\text{in}} \ll \bar{V}_{\text{in}}$.

Matrix $\langle\tilde{\mathcal{B}}\rangle$ is an expanded version of $\langle\mathcal{B}\rangle$ with the result of the linearization $\langle\tilde{\mathcal{B}_{d_\sigma}}\rangle$, i.e $\langle\tilde{\mathcal{B}}\rangle = [\langle\mathcal{B}\rangle \quad \langle\tilde{\mathcal{B}_{d_\sigma}}\rangle]$.

Classical average model

The numerical results of the linearized system (3.40) are

$$\begin{aligned} \langle\tilde{\mathcal{A}}\rangle &= \begin{bmatrix} -20 & -4 \\ 10 & -0.25 \end{bmatrix} \cdot 10^3\,, & \langle\tilde{\mathcal{B}}\rangle &= \begin{bmatrix} 10 & 22.22 \\ 0 & -1.39 \end{bmatrix} \cdot 10^3\,, \\ \langle\tilde{\mathcal{C}}\rangle &= \begin{bmatrix} 0 & 1 \end{bmatrix}, & \langle\tilde{\mathcal{D}}\rangle &= 0\,. \end{aligned} \tag{3.48}$$

General equivalent continuous model

The linearization of the system described by the matrices in (3.13) and (3.18) with (3.43), (3.44), and (3.45) is performed as proposed in Section 3.3.2 with

$\Delta_d = 1$ m, leading to the following results:

$$\langle\tilde{\mathcal{A}}\rangle = \begin{bmatrix} -18.72 & -3.83 \\ 7.17 & -1.53 \end{bmatrix} \cdot 10^3\,, \qquad \langle\tilde{\mathcal{B}}\rangle = \begin{bmatrix} 9.32 & 17.07 \\ 1.70 & 1.21 \end{bmatrix} \cdot 10^3\,, \\ \langle\tilde{\mathcal{C}}\rangle = \begin{bmatrix} 0 & 1 \end{bmatrix}, \qquad \langle\tilde{\mathcal{D}}\rangle = 0\,. \tag{3.49}$$

Fig. 3.4 shows the Bode diagram for the transfer function $V_{\text{out}}/V_{\text{in}}$ for the classical model and the general equivalent model. It is shown that the general equivalent model has a higher gain value at low frequencies but a lower one at high frequencies. Also, the classical model produces a higher phase variation raising up to 45°.

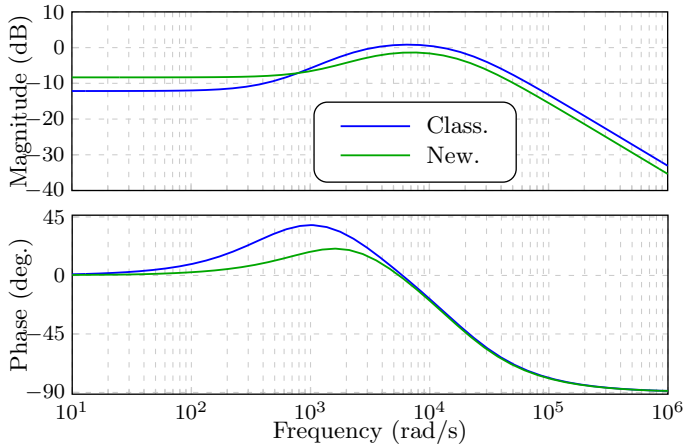


Figure 3.4: Comparison of Bode diagrams of the transfer function $V_{\text{out}}/V_{\text{in}}$

Fig. 3.5 shows the Bode diagram for the transfer function V_{out}/d for the classical model and the general equivalent model. Although the magnitude is similar, the classical model produces a higher gain noticeable at low frequencies. A remarkable difference is found in phase: notice that the classical average model has a non-minimum phase zero, and the general equivalent continuous model has minimum-phase zero almost at the same frequency. Also, the classical model has a 180° inversion. This differences affect the dynamical behavior of the system and affect the stability and performance of a closed loop control law.

3.5.4 *RMS*

See [47] in the attached papers.

3.6 Conclusion

In this chapter, a complete analytical calculation of a new equivalent continuous model and *RMS* value computation for switched systems was proposed. The models were validated with a boost power converter example showing their improvement and differences compared to the classical average model. This model can be applied to any switched system.

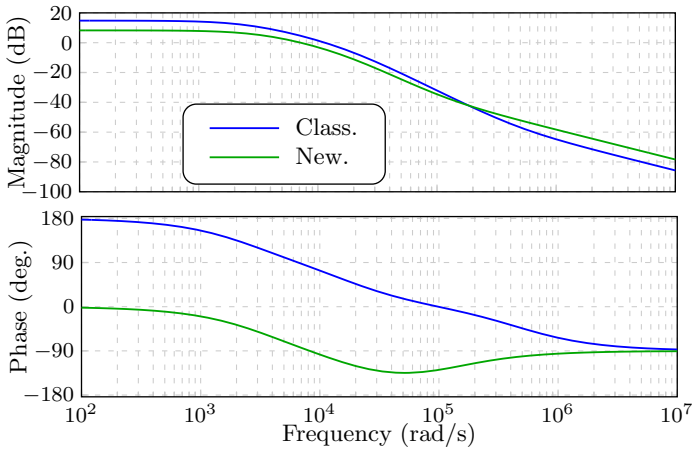


Figure 3.5: Comparison of Bode diagrams of the transfer function V_{out}/d

The proposed numerical linearization method worked well for the example exposed. On the other hand, some problems were found during the numerical computation of the model with the logarithm of A_δ on the conversion from discrete to continuous. Also, if the matrices A_n are singular, the numerical calculation of Ω_n produces some inaccuracies.

Chapter 4

Comparison of Robust Control Laws for a DC/DC Classical Ladder Multilevel Converter (CLT)

4.1 Introduction

[64], [65], [66], have designed control laws for a classical clamping- capacitors multilevel structures. However this converter requires a very complex control [62]. This chapter deals with a particular multilevel voltage elevator topology which was proposed in [50]. This converter requires less control signals, switches and capacitors compared to the other multilevel topologies. Thus, its design and control is easier. The goal of this converter is to maintain a constant voltage even if the load changes. In this chapter, robust control laws are designed considering the load as an external disturbance in the model. Moreover, the performance of the control laws are compared in simulation. The results show that the μ (DK) controller has the best response with respect to load changes. The classic PI control works better for nominal parameters. This chapter presents shortly the design of the control laws.

4.2 Classical Ladder Multilevel converter CLT

The manipulable variables of the converter (see Fig. 2.8) are: the duty cycle d, where HC_1 switches are ON the first half of the cycle (d/f_s), and HC_2 switches are their complementary, where f_s denotes the switching frequency of the converter which is constant; and the input voltage (V_{in}). The main objective of the control system is to regulate the output voltage, maintaining its value under load and operating point changes. In order to regulate the voltage, any of the two input variables mentioned above can be used.

4.2.1 Model parameters

The assumed parameters of the multilevel converter are: number of levels ($N_c = 3$); switching frequency $f_s = 50kHz$; switches ON resistances $R_{sx} = 1\Omega$; capacitors $C_x = 1\mu F$; capacitors $ESR = 1\Omega$; load resistance $R_{load} = 100\Omega$; input voltage $V_{in} = 10V$; load current I_{load}. All these values are nominal and are taken from an implemented design of a ladder multilevel converter.

4.3 Steady State Analysis

In order to decide the operational region of the converter for the control law, a steady state analysis is performed. From this analysis some conclusions about the stability and power transfer ratio of the converter are carried out and a region of operation for the control is chosen. With a state space model of the multilevel converter the relation between the input u and the output y in steady state is described by

$$\begin{aligned} 0 &= \langle A\rangle\langle x\rangle + \langle B\rangle u \\ y &= \langle C\rangle\langle x\rangle + \langle D\rangle u \end{aligned} \tag{4.1}$$

The relation y/u for different values of R_{load} was obtained as shown in Fig. 4.1. This relation is strongly dependent of R_{load}, varying the maximum gain of the converter between 0.4 and 2.7. Gains less than 1 can be achieved when the capacitors are set to a negative voltage due to the voltage drop on the resistances. However the duty cycle of maximum gain for each R_{load} is almost constant as

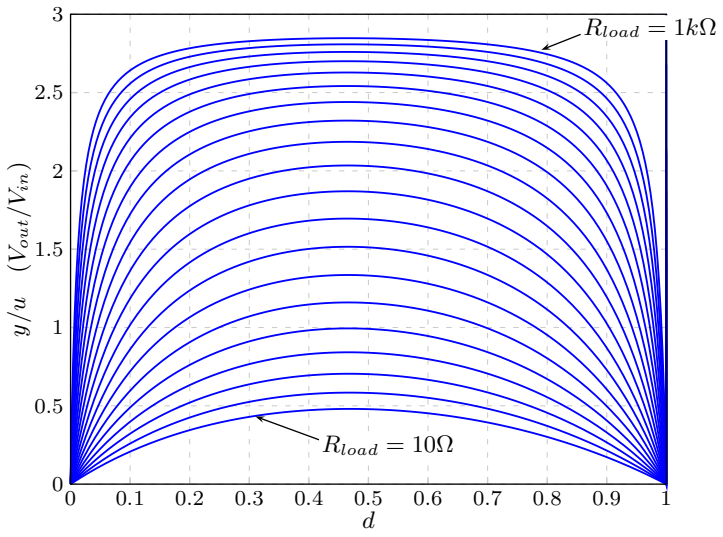


Figure 4.1: DC gain of the converter for different values of R_{load}

shown in Fig. 4.2. Due to the change in the slope sign of the converter gain after the duty cycle of maximum gain, the controller could lead to instability if that duty cycle is reached, nevertheless a high gain of the converter from y/u is needed. Therefore, work near the maximum gain point is necessary.

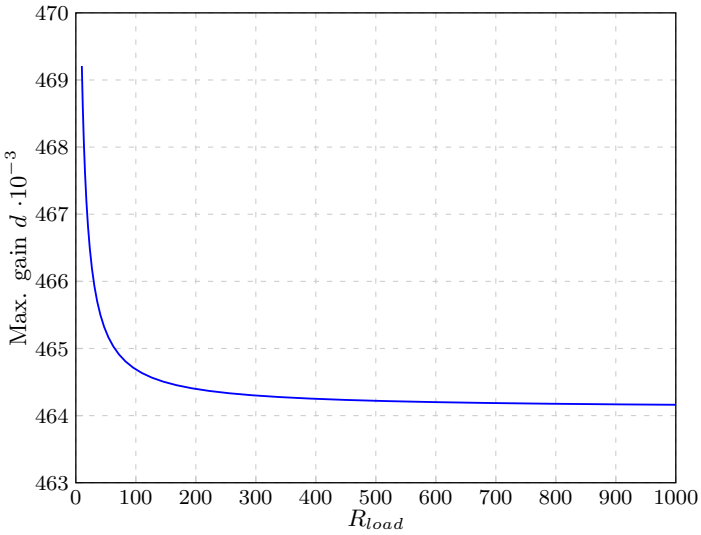


Figure 4.2: Duty Cycle of maximum gain for different values of R_{load}

Fig. 4.3 shows the power transfer ratio PTR (P_{out}/P_{in}) of the converter for different values of R_{load}. The higher PTR is found for $d < 0.5$, thus the operating point for the duty cycle is chosen to $d = 0.4$.

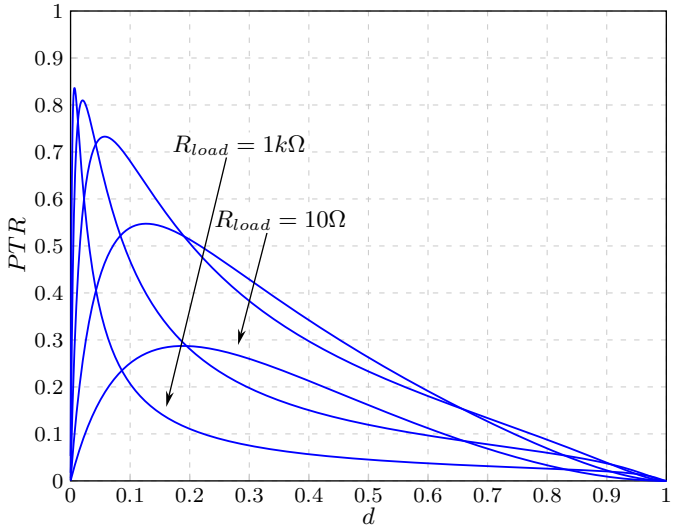


Figure 4.3: Power transfer ratio PTR (P_{out}/P_{in}) of the converter for different values of R_{load}

4.4 Masks

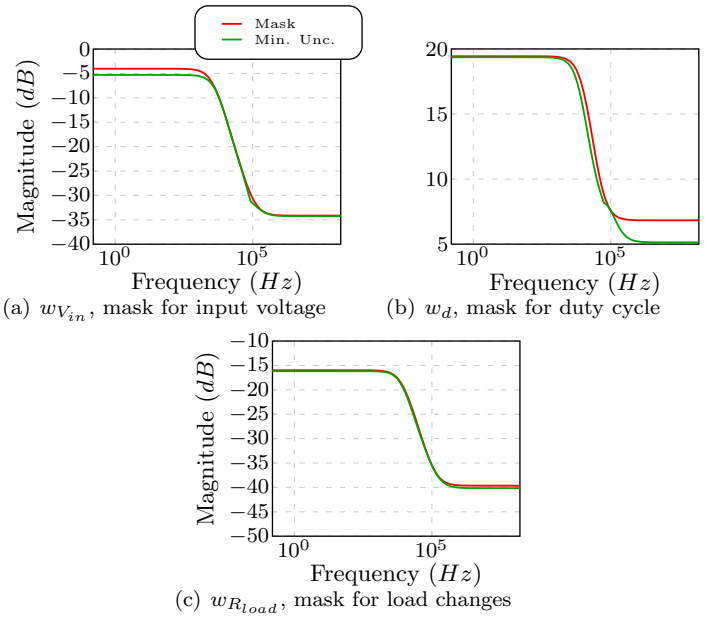
4.4.1 Uncertainty masks

Three uncertainty masks are constructed, these masks are used to consider other dynamics of the converter outside the nominal values and to design a controller that meets stability, and also performance characteristics for parameters outside nominal values.

An additive non structured uncertainty was constructed as shown in Fig. 4.5, where

$$W_1 = \begin{bmatrix} w_{R_{load}} & 0 & 0 \\ 0 & w_{V_{in}} & 0 \\ 0 & 0 & w_d \end{bmatrix}$$

$$W_2 = w_{V_{out}}$$



(a) $w_{V_{in}}$, mask for input voltage

(b) w_d, mask for duty cycle

(c) $w_{R_{load}}$, mask for load changes

Figure 4.4: Uncertainty masks W_1

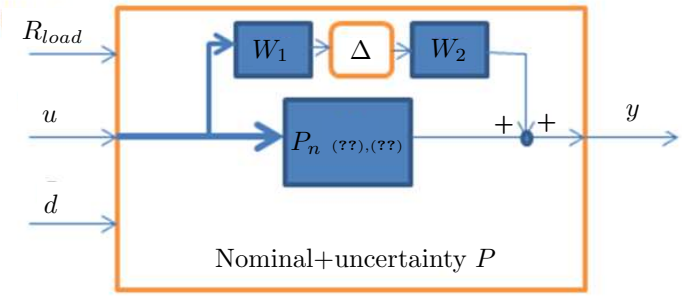


Figure 4.5: Uncertainty model P (P_n is the nominal converter)

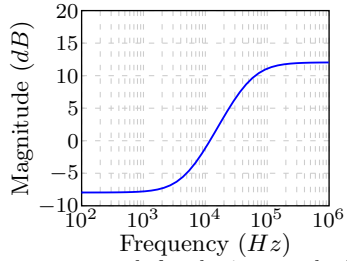
Δ is an 1x3 matrix and represents all the possible uncertainties such that $\|\Delta\|_\infty \leq 1$. In order to construct the mask W_1 the parameters R_{load}, d and V_{in} are varied over their nominal values as follows: $R_{load} = 100\Omega \pm 50\Omega$, $d = 0.4 \pm 0.06$, $V_{in} = 10V \pm 5V$.

For each mask $w_{R_{load}}$, w_{Vin} and w_d, the variation on all the parameters are taken in account. The mask w_{Vout} represents the maximum variation of the output voltage y over its regulation point and was set to $w_{Vout} = 3V$.

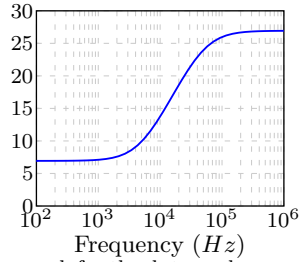
All the masks are computed taking the difference between the transfer function of the nominal converter and the converter with non-nominal values, and then, finding a 1st order transfer function that covers all the possible differences between the nominal and the non-nominal converter. The results are shown in Fig. 4.4, and show that the transfers functions y/R_{load} and y/d are considerably affected by the uncertainty, varying its gain from $-10dB$ to $20dB$.

4.4.2 Performance masks

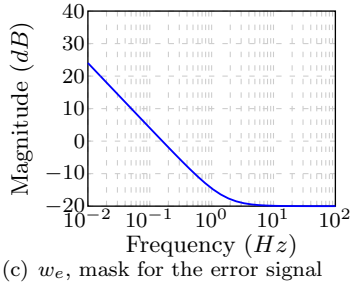
Three performance masks are used (Fig. 4.6). These performance masks are employed to get a desired response from the control signals and a small error between the output voltage an the reference voltage. Two masks are employed for the control signals that guarantee the maximum allowed amplitude (w_{d_d} and $w_{V_{in_d}}$) ($d = [0 \quad 1]$, $V_{in} = [5V \quad 15V]$) and penalize dynamics with frequencies over $f_s/10$; one more mask is employed for the error signal (w_e), that guarantees very low steady state error and neglects the high frequency ripple from the V_{out} signal.



(a) $w_{V_{in_d}}$, mask for the input voltage control signal



(b) w_{d_d}, mask for the duty cycle control signal



(c) w_e, mask for the error signal

Figure 4.6: Performance masks.

4.5 Design of the Control law

4.5.1 Classical controller

A PI controller is designed. This controller stabilizes the converter, meets a settling time less than $100ms$ and a 0 steady state error for the nominal operational conditions. The complete system structure is shown in Fig. 4.7. This controller does not guarantee performance or stability out of the nominal operational conditions since the uncertainties are not taken in to account.

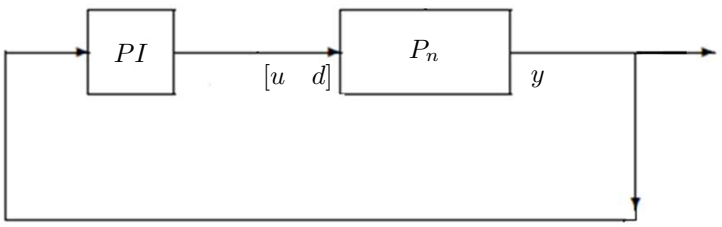


Figure 4.7: Control system structure for the PI controller

The resulting controller has the form

$$\begin{bmatrix} u(s)/e(s) \\ d(s)/e(s) \end{bmatrix}_{PI} = \begin{bmatrix} \frac{0.1985 \cdot 10^{-3} s + 12.23}{s} \\ \frac{1.388 \cdot 10^{-3} s + 28.92}{s} \end{bmatrix} \tag{4.2}$$

4.5.2 Robust controllers

The objective of a robust controller design is to take into account the behavior of the converter outside the nominal case and, for all the possible uncertainties, to guarantee stability and desired performance. Any further information in robust control theory can be found in [**?**].

The control system structure for the robust controller is described in Fig. 4.8

where K is the controller. Two controllers are synthesized; an H_∞ mixed sensitivity and a $\mu(DK)$. These controllers are both robust and consider the uncertainty.

H_∞ mixed sensitivity (H_∞ MS)

The H_∞ problem consist in find a proper, real rational controller K that stabilizes G internally and minimizes the H_∞ norm from w (perturbations) to z (performance measurement) $(min\|T_{zw}\|_\infty)$, where T_{zw} is the transfer function form w to z. See Fig. 4.9

There exists a controller K_{sub} such that $\|T_{zw}\|_\infty < \gamma$,γ is a constant, with the form

$$K_{sub} = \begin{cases} \dot{k} = A_\infty k + B_\infty y \\ u = C_\infty k \end{cases} \tag{4.3}$$

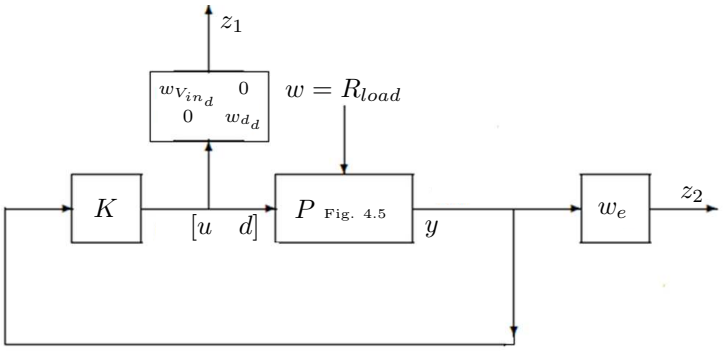


Figure 4.8: Complete control system, K represents the controller, w_e, $w_{V_{in_d}}$ and w_{d_d} are performance masks. w is an external perturbation and, z_1 and z_2, are performance measurements

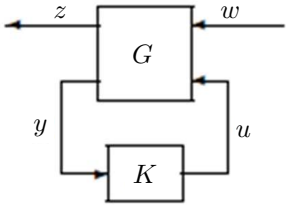


Figure 4.9: Block diagram of the extended converter G and the controller K

Where A_∞, B_∞ and C_∞, are the solutions given by the H_∞ algorithm. This is a suboptimal controller since the optimal solution is numerically an theoretically complicated.

The H_∞ MS problem includes the uncertainty and uses the H_∞ algorithm, reducing the H_∞ norm from w and w_Δ to z and z_Δ as a non structured case as shown in Fig. 4.10.

The synthesized controller is 10^{th} order and met nominal performance and robust stability. The results of the H_∞ MS controller synthesis are shown in Table 4.1.

A balanced reduction of the controller to 5^{th} and 1^{st} order are evaluated (Fig. 4.11), in both cases the robust stability and nominal performance are maintained. Moreover, the numerical results of the indexes in Table 1 are practically the same for the full order controller and its reductions.

The transfer function of the 1^{st} order reduction of the H_∞ MS controller is

$$\begin{bmatrix} u(s)/e(s) \\ d(s)/e(s) \end{bmatrix}_{H_\infty MS} = \begin{bmatrix} \frac{33.61 \cdot 10^{-3} s + 9.186}{s + 10^{-4}} \\ \frac{0.2447 \cdot 10^{-3} s + 0.1092}{s + 10^{-4}} \end{bmatrix} \tag{4.4}$$

μ DK controller

The μ problem consist in finding a controller K that minimizes the structured singular value form w and w_Δ to z and z_Δ (Fig. 4.10). In contrast to the H_∞

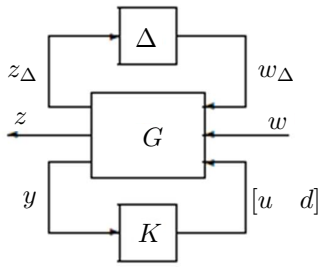


Figure 4.10: Block diagram of the extended converter G and the controller K with the uncertainty Δ

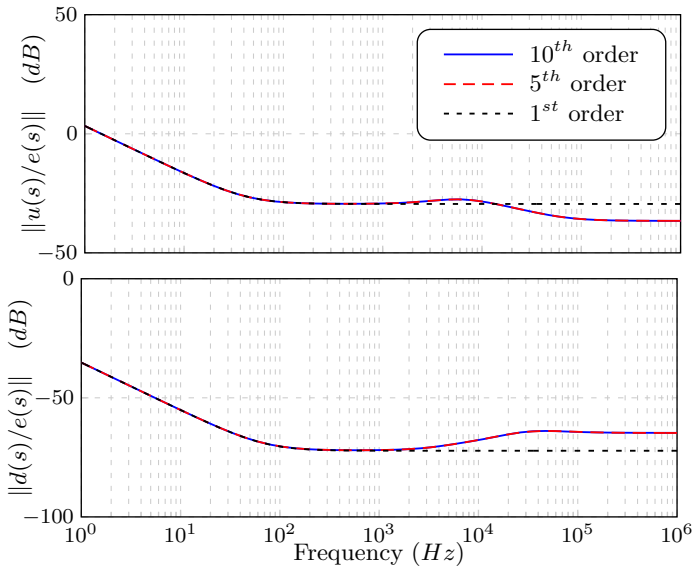


Figure 4.11: Bode diagram of the H_∞ MS controller and its reductions.

MS case, there is no relation between, z_Δ and w, and , z and w_Δ, leading to a less conservative analysis.

The resulting controller was 16^{th} order and does not meet robust performance, however the controller guarantees robust stability and nominal performance.

Again, a balanced reduction of the controller to 5^{th} and 1^{st} order was evaluated (Fig. 4.12) maintaining robust stability and nominal performance. The numerical results of the indexes in Table 4.1 are practically the same for the full order controller and its reductions.

The transfer function of the 1^{st} order reduction of the μ DK controller is

$$\begin{bmatrix} u(s)/e(s) \\ d(s)/e(s) \end{bmatrix}_{\mu(DK)} = \begin{bmatrix} \frac{-5.165 \cdot 10^{-3} s + 20.52}{s + 10^{-4}} \\ \frac{-0.9087 \cdot 10^{-3} s + 0.674}{s + 10^{-4}} \end{bmatrix} \tag{4.5}$$

The results obtained in Table 4.1 show that the PI controller only satisfies nominal performance as expected. However, the two robust controllers fulfill

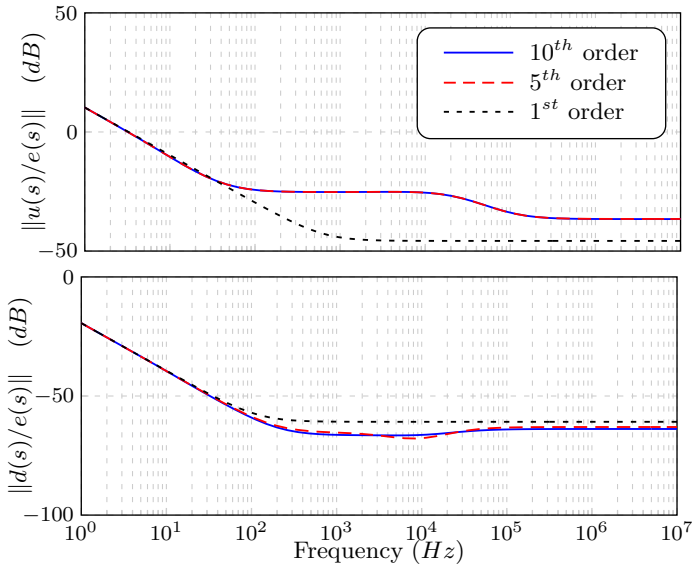


Figure 4.12: Bode diagram of the μ DK controller and its reductions.

Table 4.1: Controller order an indexes comparison, an index lower than 1 indicates that the controller fulfill the requirement.

Controller	Order	Rob. stab.	Nom. perf.	Rob. perf.
PI	1	3.001	0.901	4.254
H_∞ MS	10, 5, 1	0.964	0.714	2.766
μ DK	16, 5, 1	1.015	0.677	2.707

the requirement of nominal performance too and moreover, they are robustly stable as well. The μ (DK) controller has lower indexes than H_∞ MS in the nominal performance and robust performance, that means it has a better response. However, the H_∞ MS controller has a better stability index but still both are robustly stable. Since the μ (DK) controller is less conservative it is expected that has lower indexes than the H_∞ MS and still be robustly stable.

None of the controllers fulfills the robust performance requirement. However, the μ (DK) controller has the better response.

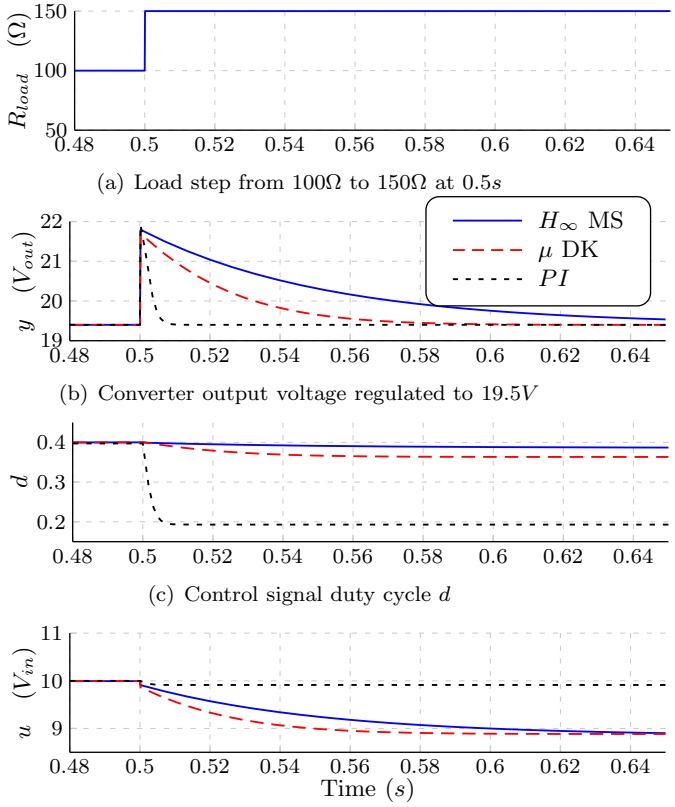
4.6 Simulation Results

The three controllers are compared on a simulation over the nonlinear average model. Two cases are evaluated with a step perturbation of $+/-50\Omega$ of the load resistance over its nominal value. The results are shown in Fig. 4.13 and Fig. 4.14. It can be concluded that the H_∞ MS and μ (DK) controllers are robustly stable and the μ (DK) controller has a faster response than the H_∞ MS controller.

For this simulation both control signals are bounded, the duty cycle d between 0 and 1; and the input voltage V_{in} between $0V$ and $30V$.

4.6.1 Load perturbation $+50\Omega$

A load perturbation from 100Ω to 150Ω is applied. Fig. 4.13 shows the response of PI, H_∞ MS and μ (DK) controllers. All the controllers are stable for this load perturbation. The PI controller has the fastest response, furthermore, the PI and μ (DK) controllers use a higher amplitude of the duty cycle control signal in order to regulate the output voltage. The H_∞ MS controller nevertheless, uses less amplitude in the duty cycle control signal and almost the same V_{in} input voltage of the μ (DK) controller with the slowest time response.



(a) Load step from 100Ω to 150Ω at $0.5s$

(b) Converter output voltage regulated to $19.5V$

(c) Control signal duty cycle d

(d) Control signal input voltage V_{in}

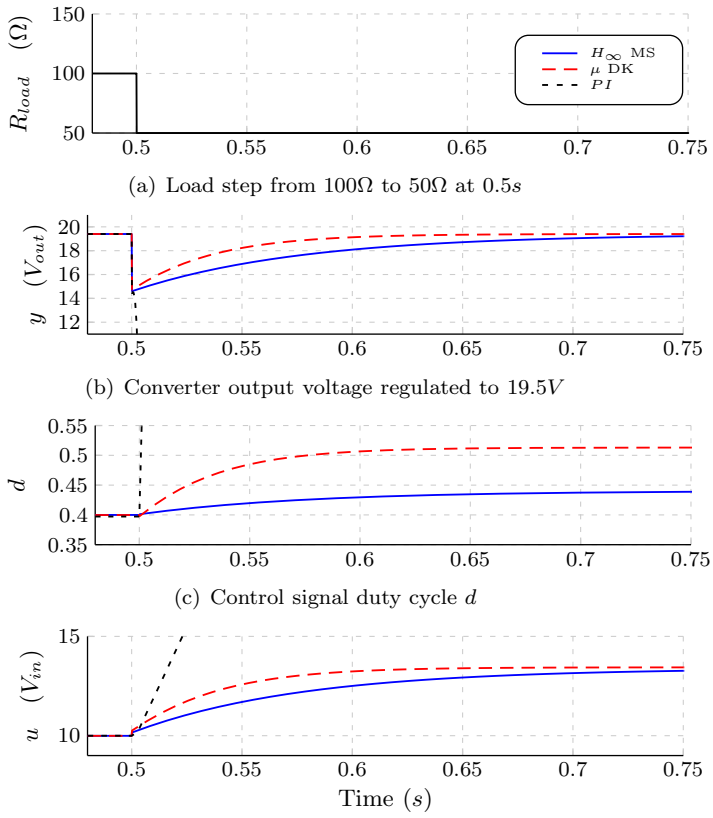
Figure 4.13: Response to a load perturbation of PI, H_∞ MS and μ (DK) controllers.

4.6.2 Load perturbation -50Ω

A load perturbation from 100Ω to 50Ω is applied. Fig. 4.14 shows the response of PI, H_∞ MS and μ (DK) controllers. The PI controller is clearly unstable for this perturbation; this instability is mainly due to the change of phase and gain augmentation in the y/d transfer function near the duty cycle of maximum

gain as shown in Fig. 4.1 and Fig. 4.3. The PI controller uses d more than V_{in} in order to correct the output voltage, reaching the point of maximum gain of y/d too fast. Furthermore, the V_{in} control signal is not fast enough to correct the error leading to the system instability.

The H_∞ MS and μ (DK) controllers consider the converter uncertainties, and both are stable to the load perturbation as expected. However the μ (DK) analysis is less conservative than the H_∞ MS giving to μ (DK) controller better performance maintaining its robustness.



(a) Load step from 100Ω to 50Ω at 0.5s

(b) Converter output voltage regulated to 19.5V

(c) Control signal duty cycle d

(d) Control signal input voltage V_{in}

Figure 4.14: Response to a load perturbation of PI, H_∞ MS and μ (DK) controllers.

4.7 Conclusions

In this chapter a dynamic and static model of a multilevel converter was analyzed, the conventional average model showed a poor performance in order to model the converter for the given values of capacitors and resistances; however the dynamics were too similar. The controllers showed that in order to meet robust stability, an analysis including the system uncertainties was needed and therefore, an uncertain model of the converter was required. An H_∞ MS method and a μ (DK) synthesis were required to meet robust stability, and the

μ (DK) controller had better time response than the H_∞ MS but with a greater order, however the balanced reductions showed to maintain the robustness and performance indexes reducing the controller even to 1^{st} order.

Chapter 5

Ladder Multilevel Converter Analysis Using a New Equivalent Continuous Model

5.1 Introduction

In a switched capacitor converter, capacitors with different voltages can be connected producing current spikes. Since the ESR of the capacitors and the ON resistance of the interconnection switches are usually small the equivalent time constant τ of the resulting circuit is also small therefore the dynamics are rapid compared to the switching period (see Fig. 5.1). Due to the rapid dynamics of the current of the capacitors the assumption for the classical average model is not fulfilled. In chapter 3 a new analytical modeling technique that allows to obtain an equivalent continuous model of a switched converter regardless the dynamics on each switching state is proposed. In this chapter this technique is used in order to analyze the behavior of the converter and optimize its efficiency.

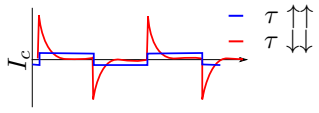


Figure 5.1: Current waveform for different τ values

It can be seen in Fig. 5.1 that for small τ (i.e. small ESR and switches ON resistance) the current waveform presents an exponential shape and higher current spikes than for greater τ values (i.e. higher ESR and switches ON resistance). Moreover, due to charge balance, both waveforms must have the same average en each cycle. Since the average is the same it can be concluded that the exponential waveform has a higher RMS value. Notice how reducing the resistor value implies the increase in the RMS and, since the power losses

are given by $\|i\|^2_{RMS}R$, no conclusion about the power losses in the resistor can be made easily.

In [22], [67], [20], [18], [19], [23] power losses in switched capacitor converters are treated an analyzed. It is mentioned that in SC converters reducing the ON resistance of the switches or the ESR not necessarily implies higher efficiency. In this chapter a different approach to the converter analysis and optimization is addressed using a new averaging technique applied to a design problem of a DLT converter with eight cells for high voltage application. The components of the converter are chosen to optimize its efficiency. Moreover, the converter is implemented and experimental measurements are taken.

5.2 CLT Analysis

In this section the model obtained with the classical technique is compared with the model obtained with the generalized continuous technique and some conclusions about the behavior of the CLT are carried out.

Fig. 5.2 shows a comparison of the step response of the two modeling methods with the switched system in simulation. It is clear that with the classical model an inaccurate DC gain is obtained. The new method however, seems to be accurate and is able to obtain a correct value of the DC gain.

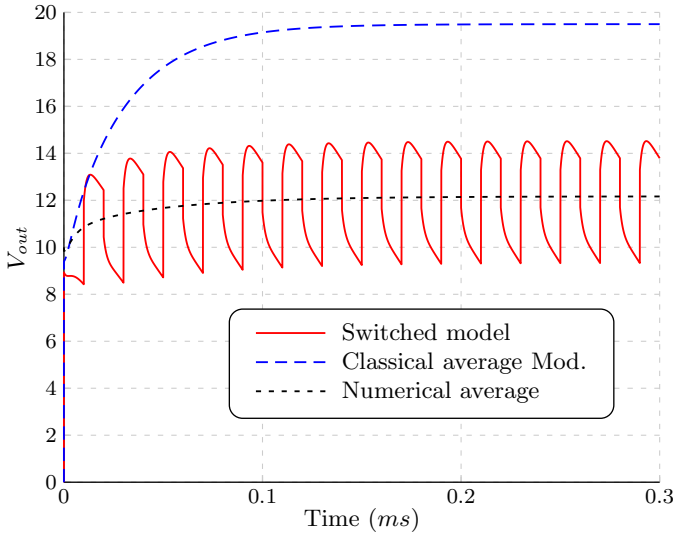


Figure 5.2: 10V step response of the converter of V_{out}/V_in for the nominal conditions, with $d = 0.4$ and $R_{load} = 100\Omega$

In power converters it is common to use the duty cycle in order to control the output variable. Fig. 5.3 shows a comparison of the DC gain of the converter for different duty cycles using the two models. The differences on the DC gain mentioned before can be noticed now for different duty cycles; a maximum gain near 2 is obtained with the classical model and a maximum gain near 1.3 is obtained with the new model. These differences are mainly due to the fast dynamics of the converter on each switching state. In order to apply the

classical average model and obtain an accurate results these dynamics must be slow. Another noticeable difference is the duty cycle of maximum gain, for the classical model is near $d = 0.47$ and for the new model is near $d = 0.3$ (see chapter 4).

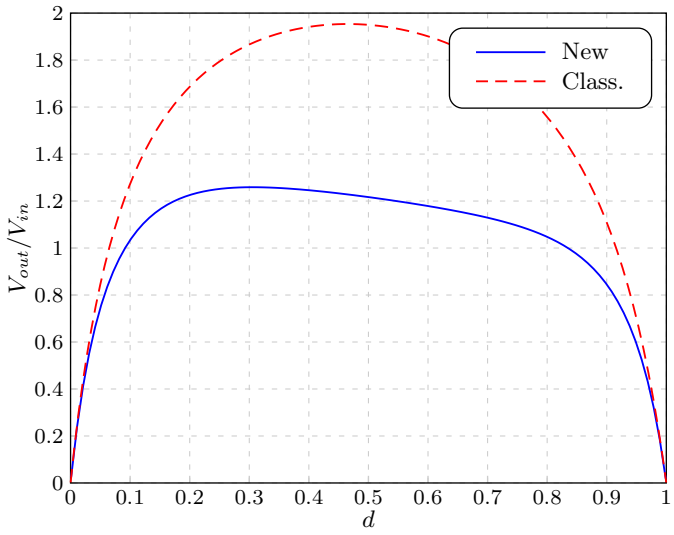


Figure 5.3: Comparison of the DC gain of the converter V_{out}/V_{in} for $R_{load} = 100\Omega$ with the two models

Fig. 5.4 shows the DC gain of the converter using the new model and for different resistive load values. It can be seen how the gain of the converter V_{out}/V_{in} varies from more than 2.5 for small loads to less than 0.5 for bigger load which limits the regulation capabilities of the converter if only the duty cycle is used as control signal. Moreover, the duty cycle of maximum gain is dependent on the load, making it difficult to obtain the maximum gain of the converter in a practical situation. Fig. 5.5 shows how the duty cycle of maximum gain varies with the load resistance. Moreover, this duty cycle varies with the switching frequency of the converter.

Since the input voltage source V_{in} is analyzed with zero output resistance the duty cycle of maximin gain is in all cases different form 0.5 and varies with load changes.

A comparison of the frequency response of the converter with the two models is shown in Fig. 5.6. The difference of the DC gain is noticed in de magnitude plot. Furthermore, the differences on the phase plot show than the pole and zero are closer than in the classical model producing a different time response.

The analysis shows an inaccuracy of the classical model due to the fast dynamics of the converter on each switching state. However, the new method is able to model correctly the SC converter since it is not dependent of the switching states dynamics.

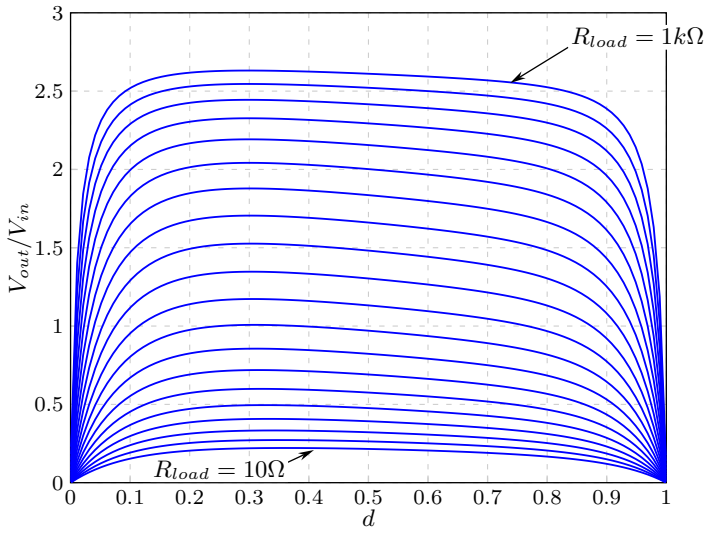


Figure 5.4: DC gain of the converter V_{out}/V_{in} using the new average model

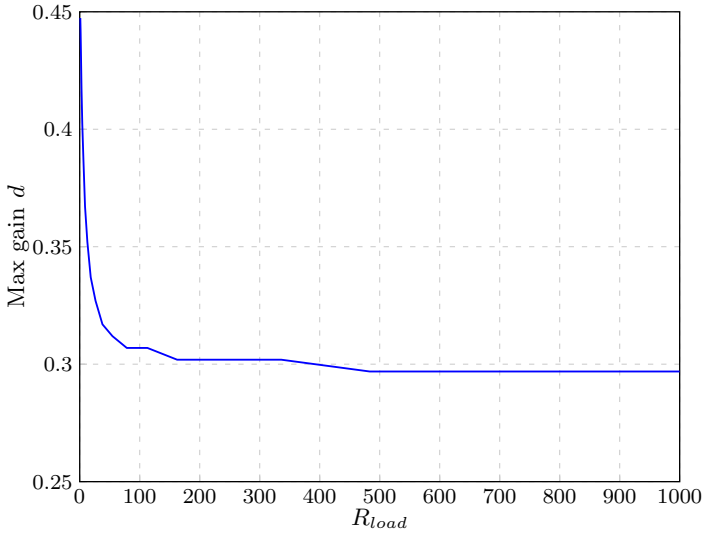


Figure 5.5: Duty cycle of maximin gain of the converter for different values of R_{load}

5.3 DLT Analysis

Since the new modeling technique is able to model accurately the SC converter, it is used to analyze and optimize the DLT for further implementation.

The nominal values of the converter are: input voltage $V_{in} = 350V$; output voltage $V_{out} = 3000V$; output current $I_{out} = 100mA$; number of cells $N_c = 8$. Since the capacitors voltage must be rated at least $400V$ and they must be physically small, a commercial value $C = 2.2\mu F$ is chosen.

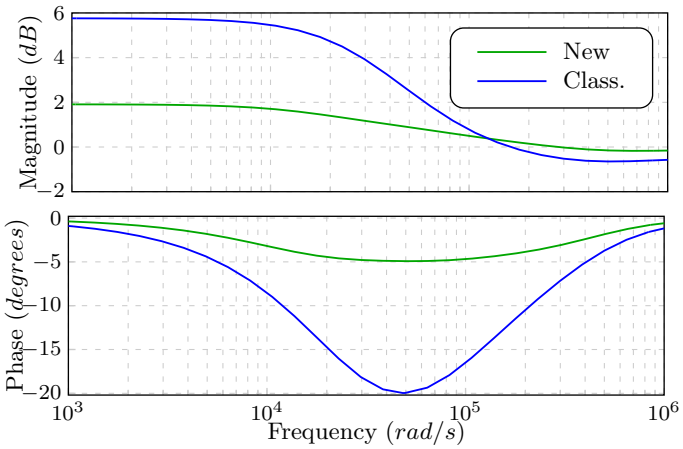


Figure 5.6: Bode diagram comparison of V_{out}/V_{in} for the two models

5.3.1 Duty Cycle of maximum gain

The DC gain of the converter as a function of the duty cycle d for different load values is shown in Fig. 5.7. As a main difference with CLT it can be seen that the duty cycle of maximum gain is independent of the load value and is always $d = 0.5$. Moreover, this value of duty cycle is independent of the switching frequency of the converter. This is another advantage not mentioned in chapter 2 respect to CLT if a maximum gain is desired.

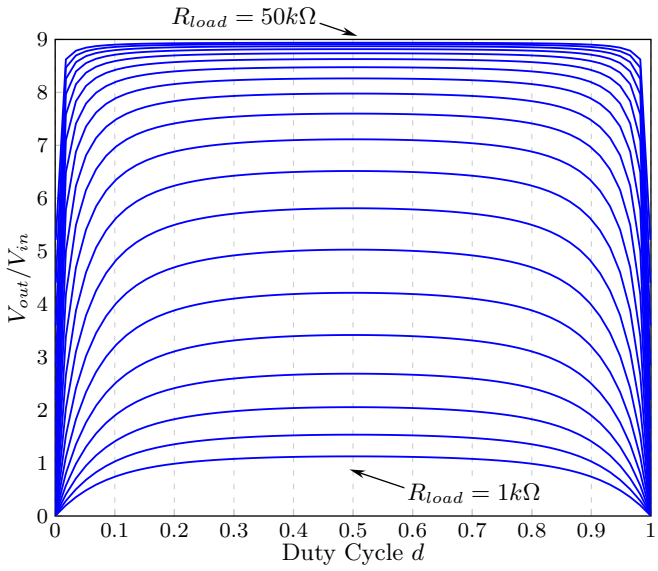


Figure 5.7: Voltage gain V_{out}/V_{in} of a DLT with $N_c = 8$ for different values of resistive load

5.3.2 Efficiency

As it is mentioned before, an easy conclusion about the efficiency can not made due to the effect on the current waveform when the resistances are small. In Fig. 5.8 the efficiency of the converter as a function of the capacitor ESR R_C and the switches ON resistance R_S is shown. The higher efficiency (lighter zone) is not obtained with the lower resistance values; actually, for these values the efficiency is under 50%. However, for values near $R_C = 1.3\Omega$ and $R_S = 3.1\Omega$ efficiency is up to 96.9%.

The resistance R_C affects the efficiency more than R_S, notice how for greater values of R_C the region is darker (lower efficiency). This effect is due to the current distribution in the converter (see Fig. 2.8)

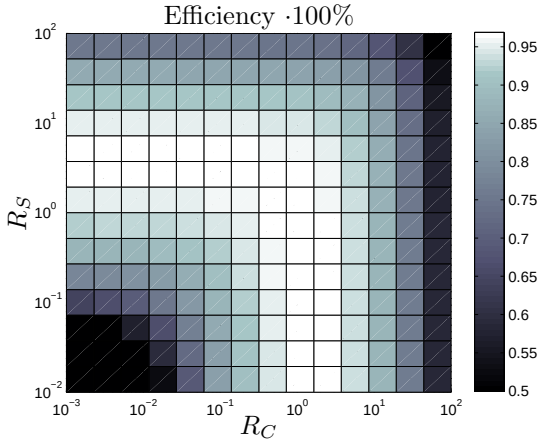


Figure 5.8: Efficiency of DLT for different values of capacitor ESR (R_C) and switches ON resistance (R_S) at a switching frequency $f = 75kHz$. (Max efficiency 96.9%)

When a lower frequency is used, the efficiency (only conduction losses) is reduced. Fig. 5.9 shows the difference of the efficiency obtained for two switching frequencies $f = 50kHz$ and $f = 75kHz$. Notice how all the values are negative which means a reduction of the efficiency. For the higher efficiency points of Fig. 5.8, Fig. 5.9 shows a reduction of the efficiency around 1.5%. The highest efficiency reduction can be found for low resistance values; for these values the efficiency of Fig. 5.8 is already low (near 50%).

Fig. 5.10 shows the output resistance of the DLT with $f = 75kHz$. Notice how for $R_C < 3.5\Omega$ and $R_S < 10\Omega$ R_{out} stabilizes near 580Ω. Nevertheless, the efficiency of Fig. 5.8 varies on this region. Comparing Fig. 5.8 and Fig. 5.10 it can be seen that the higher efficiency is reached near the point where the output resistance R_{out} of the converter begin to stabilize.

When the switching frequency is reduced the output resistance R_{out} is incremented as shown in Fig. 5.11. Notice how near the points of maximin efficiency R_{out} is incremented in around 250Ω.

Since the current ripple through the capacitors is more than $1A$ due to current spikes, a low ESR is preferred. A commercial capacitor with $C = 2.2\mu F$ and $R_C = 2.5m\Omega$ is chosen. Therefore, R_S and f will be chosen in order to

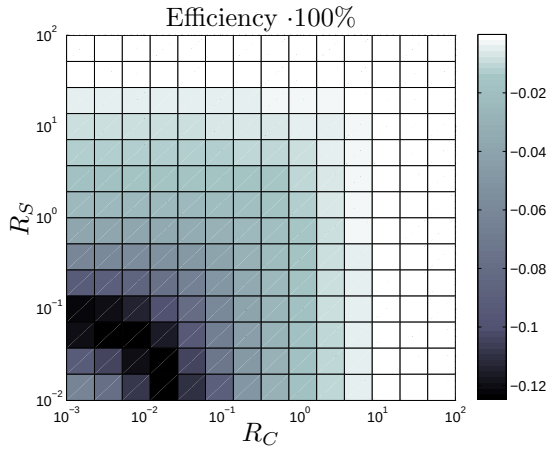


Figure 5.9: Efficiency difference for different values of capacitor ESR (R_C) and switches ON resistance (R_S) at a switching frequency of $f = 50kHz$ respect of the efficiency at $f = 75kHz$; negative values means a decrement of the efficiency at $50kHz$

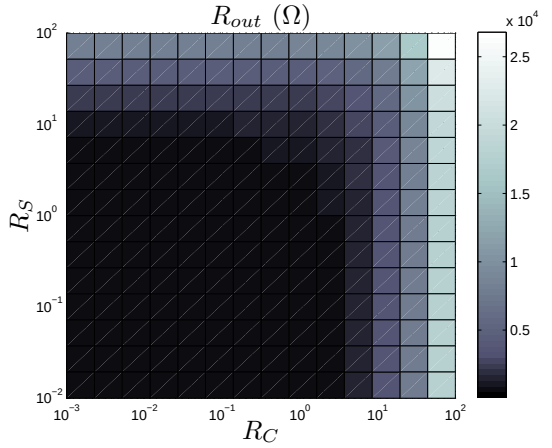


Figure 5.10: Output resistance R_{out} of DLT for different values of capacitor ESR (R_C) and switches ON resistance (R_S) at a switching frequency $f = 75kHz$. (Min $R_{out} = 580\Omega$)

optimize the efficiency.

In Fig. 5.12 the efficiency for different values of R_S and f is shown. It can be seen that the efficiency is higher for higher frequency values (conduction losses only). Due to hardware limitations, the highest frequency that can be obtained is $f = 75kHz$; for this frequency the values of R_S that are nearest the highest efficiency point are $1.7\Omega < R_S < 6.3\Omega$. A commercial N-MOS transistor P8NK100Z with $R_S = 1.8\Omega$ is chosen resulting in a theoretically efficiency of 96%.

It can be seen in Fig. 5.13 how the lowest output resistance (lighter zone) not necessarily means higher efficiency (see Fig. 5.12). For the selected resistance

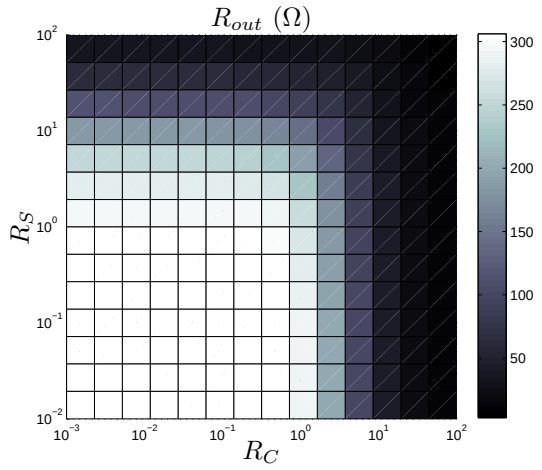


Figure 5.11: Output resistance R_{out} difference for different values of capacitor ESR (R_C) and switches ON resistance (R_S) at a switching frequency of $f = 50kHz$ respect of the output resistance at $f = 75kHz$; positive values means an increment of the resistance at $50kHz$.

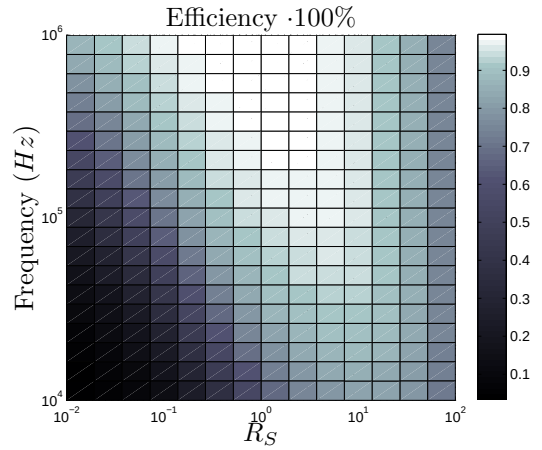


Figure 5.12: Efficiency of DLT for different values of switching frequency (f) and switches ON resistance (R_S) with $C = 2.2\mu F$ and $R_C = 2.5m\Omega$. (Max efficiency 99.2%)

values, an output resistance $R_{out} = 790\Omega$ is obtained.

Fig. 5.14 shows a comparison of the efficiency for the selected switch $R_S = 1.8\Omega$ an other with $R_S = 0.18\Omega$. Clearly a higher efficiency is obtained with $R_S = 1.8\Omega$ for frequencies $f < 800kHz$. Above $f = 800kHz$ the switch with $R_S = 0.18\Omega$ presents higher efficiency. However, this analysis only takes into account the conduction losses, at $f = 800kHz$ the switching losses can become very high and the efficiency can be reduced.

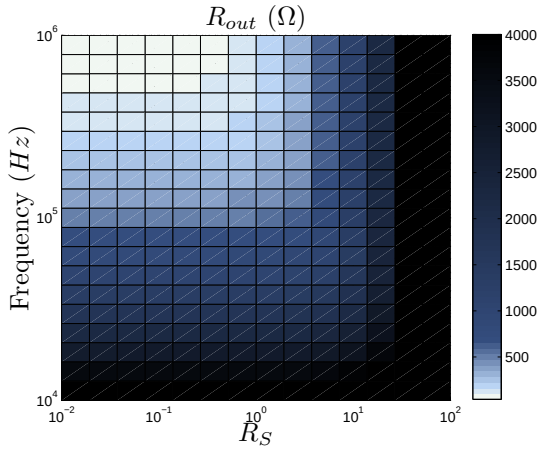


Figure 5.13: Output resistance R_{out} of DLT for different values of switching frequency (f) and switches ON resistance (R_S) with $C = 2.2\mu F$ and $R_C = 2.5m\Omega$. (Min $R_{out} = 58\Omega$)

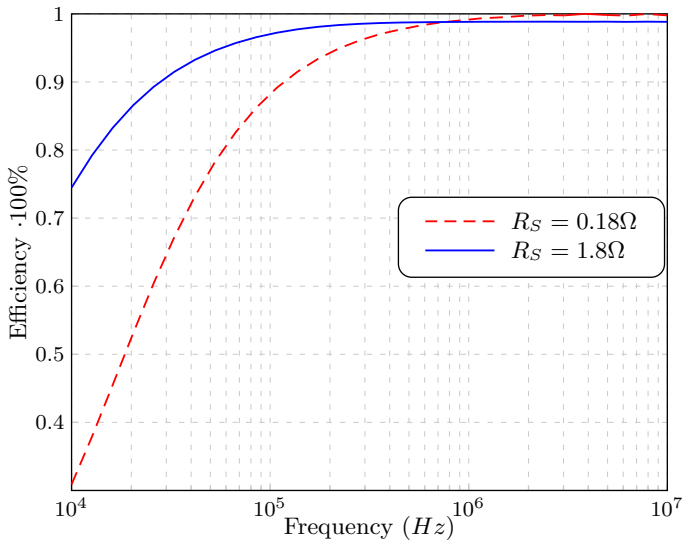


Figure 5.14: Efficiency comparison for different values of switches ON resistance R_S with $C = 2.2\mu F$ and $R_C = 2.5m\Omega$

5.3.3 Duty Cycle effect

With the selected parameters, the variation of the converter gain V_{out}/V_{in} with the duty cycle d is shown in Fig. 5.15. This variation is not significant and therefore the duty cycle can not be used as control signal. Since all the switches control signals are driven by pulse transformers as in [46], [44] and the duty cycle of maximum gain is constant and equal to 0.5 this value is chosen for the converter implementation.

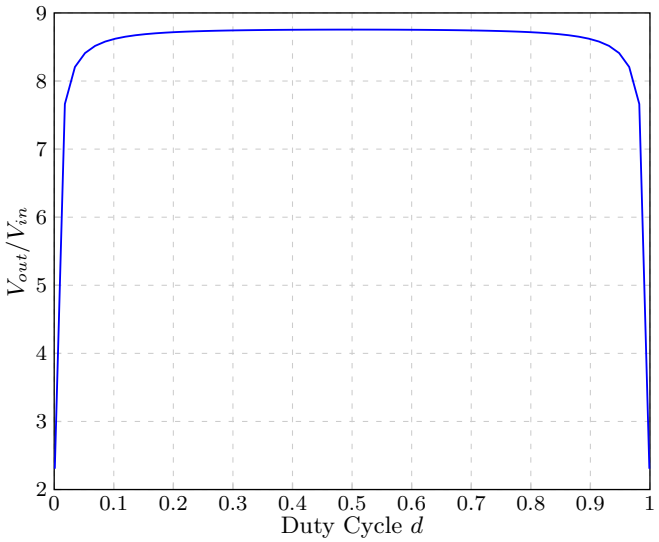


Figure 5.15: Voltage gain V_{out}/V_{in} of a DLT with nominal values (i.e. $N_c = 8$, $R_S = 1.8\Omega$, $C = 2.2\mu F$, $R_C = 2.5m\Omega$, $f = 75kHz$.

5.3.4 Converter implementation

The final nominal values of the parameters chosen for the implementation of the converter are shown in Table 5.1

Table 5.1: Converter parameters

DLT converter	
N_C	8
V_{in}	0-350V
V_{out}	0-3000V
I_{out}	0-100mA
Switch	N-MOS P8NK100Z
R_S	1.8Ω
C	2.2μF
R_C	2.5$m\Omega$
f	75kHz
d	0.5

5.4 Experimental Results

In order to validate the theoretical analysis, experimental measurements are taken. Table 5.2 shows a comparison between theoretically and experimental efficiency. The experimental efficiency was measured at 300W (i.e. $V_{out} = 3000V$ and $I_{out} = 100mA$).

Table 5.2: Comparison of theoretical and experimental efficiency

	$20kHz$	$50kHz$	$75kHz$
Theoretical	87%	93.5%	96%
Experimental	84.5%	90.5%	92%

The results show a difference on the efficiency up to 4% at $75kHz$. This difference is mainly attributed to switching losses since they are not taken into account on the analysis carried out in this chapter. However, The higher efficiency is achieved at $75kHz$ as expected.

5.5 Conclusions

In this chapter, CLT was analyzed using different modeling techniques. The classical average model shows poor accuracy modeling the converter. Therefore, a new modeling technique is used. It was showed that the duty cycle of maximum gain of the CLT is dependent with the load and the frequency.

The DLT was analyzed with the new model and the optimal parameter values was founded. These parameters were subjected to constraints of hardware and commercial components. Thus, higher efficiencies could be achieved. It was shown that the highest efficiency is not achieved necessarily with the smallest resistor values and it is strongly dependent on the frequency; therefore, a careful analysis is needed in order to obtain the highest efficiency point.

Since the analysis carried out did not take into account the switching losses the experimental results are different from the theoretical. However, the increase of the switching losses at $75kHz$ were low enough to maintain this frequency with high efficiency. For higher frequency values the switching losses can become more important.

Chapter 6

Modeling and Control Design of a Double Ladder Multilevel Converter for a Glow Discharge Application

6.1 Introduction

When the system does not satisfy the suppositions of the modeling technique, an inaccurate model is obtained. In chapter 4, several control laws are designed for a ladder multilevel converter using the classical average model [53]. However, the poor accuracy of this modeling technique for this particular converter leads to a degraded performance of the control law on the switched converter. In this work the inaccuracy of the classical average technique is verified. Moreover, the technique from chapter 3 is evaluated and validated with accurate results on a converter in double ladder topology (DLT) proposed in chapter 2. Finally, a robust control law is designed an implemented in a NI cRIO FPGA module for a $3000V$, $100mA$ glow discharge application. Its performance is tested experimentally.

6.2 Robust Control Design

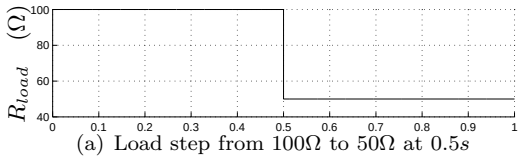
6.2.1 Classical average model problem

In chapter 4 three control laws to regulate the output voltage were designed for the CLT, two robust controllers using $H_\infty Mixed Sensitivity$ and synthesis μ_{DK}, and a classical PI. For the controllers design the classical average model is used.

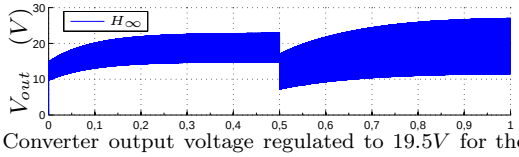
The performance of the controllers to a load perturbation at $t = 0.5s$ is tested in simulation with the nonlinear classical average model and the results are shown in Fig. 4.14. It can be seen that the three controllers are stable for the nominal case, and only the robust controllers are stable to the load perturbation.

In Fig. 6.1 the performance of the controller is tested on the switched model. For this case the robust controllers are stable for the nominal case. Nevertheless only the $H_\infty MixedSensitivity$ is stable for the load perturbation. The PI controller is unstable for the nominal case.

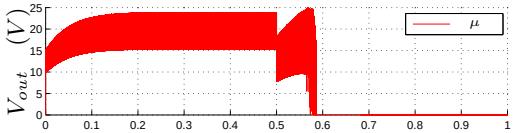
Notice that the control signals for both controllers using the switched model (Fig. 6.1) have higher amplitude than the control signals with the averaged model (Fig. 4.14).



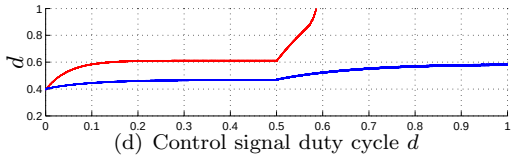
(a) Load step from 100Ω to 50Ω at $0.5s$



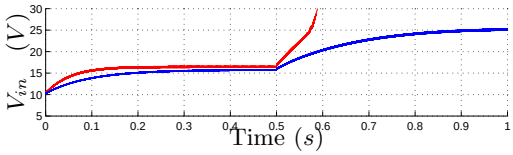
(b) Converter output voltage regulated to $19.5V$ for the H_∞ MS controller



(c) Converter output voltage regulated to $19.5V$ for the μ (DK) controller



(d) Control signal duty cycle d



(e) Control signal input voltage V_{in}

Figure 6.1: Response of the robust controllers on the switched converter

The response obtained for both simulations shows that the controllers performance is as expected since they are designed using the classical averaged model (Fig. 4.14). However, in the switched case the performance is clearly different. Fig. 5.2 shows the step response of the classical averaged model and the switched system. It can be seen clearly that the averaged model does not represent accurately the dynamics of the converter, and can not be used in order to design control laws in this case.

6.2.2 Glow discharge control using the General Equivalent Continuous Model

The main objective of the control law is to start-up and regulate the current of a glow discharge generated at atmospheric pressure.

System Description

Due to the advantages of the DLT topology, this is used for the final implementation. The structure of the system is shown in Fig. 6.2. The system consists in a buck-boost converter, a ladder multilevel converter (DLT) and an external load. The buck-boost controls the input voltage to the multilevel converter using its duty cycle d_{BB}. The multilevel converter boost the output voltage of the buck-boost to a higher DC level (up to $3000V$).

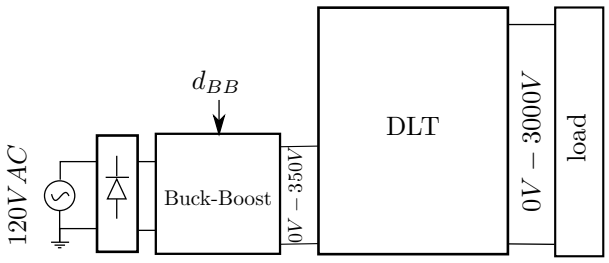


Figure 6.2: System scheme

The load is shown in Fig. 6.3. The glow discharge is generated between two electrodes at atmospheric pressure with a maximum current of $100mA$. L_{load} and R_{load} are used to limit the the load current when the discharge occurs. The

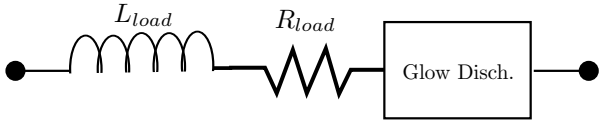


Figure 6.3: Load description

glow discharge is modeled as a voltage source.

For the control design the variables taken into account are: the controlled variable is the current through the load I_{load}, this current is the same as for the glow discharge; the control variable is the duty cycle of the buck-boost converter d_{BB}, which modifies the output voltage of the buck-boost and therefore, the output voltage of the DLT.

Performance measurement

Two performance measurements are used. One for the error signal (difference between the desired output current and the actual output current) which guarantees high frequency rejection, typically noise due to the switching frequency, and low steady state error. Another performance measurement is used for the control signal d_{BB} which guarantees dynamics only of frequencies ten time lower

than the buck-boost switching frequency and limits the amplitude of the control signal between 0 and 1.

6.3 Implementation

A buck-boost and a DLT converter are implemented as shown in Fig. 6.2. The buck-boost controls the input voltage of the DLT between $0V$ and $350V$ using its duty cycle d_{BB}. For its implementation bidirectional switches are used (NMOS SPP17N80C3) with an external antiparallel diode and a blocking diode (C4D02120A). Finally, an inductance $L_{BB} = 100\mu H$ and an output capacitor $C_{BB} = 6.6\mu$ are used with a switching frequency $f_{BB} = 100kHz$.

The DLT was implemented as shown in Fig. 2.8. For its implementation eight cells are used $N_c = 8$ leading to a maximum output voltage $V_{out} = 3000V$. A NMOS P8NK100Z with ON resistance $R_s = 1.8\Omega$ and capacitors $C_x = 2.2\mu F$ with ESR $R_C = 2.5m\Omega$ are employed. The converter uses a switching frequency $f_{DLT} = 75kHz$ with a constant duty cycle $d_{DLT} = 0.5$. In order to drive the gate control signals for this converter insolated pulse transformer are used. The load parameters of Fig. 6.3 are: $R_{load} = 25k\Omega$ and $L_{load} = 10H$.

For the implementation of the controller a NI-CRio9022 is used, this controller has an internal FPGA running at $40MHz$. To manage the input an output signals two I/O digital modules (NI 9401 and NI 9403) are employed. The analog input signals are acquired with a NI 9201 module with a sample rate of $500KS/s$.

Since the $\mu(DK)$ controller provides better performance than the $H_\infty MS$ with the same robust stability as shown in chapter 4, only this controller is implemented and tested on the glow discharge.

6.4 Experimental Results

6.4.1 Model Validation

In order to validate the modeling technique presented in chapter 3, experimental measurements are taken for the implemented DLT converter. In Fig. 6.4 the experimental step response is compared with the model obtained with the classical average method, the results show clearly the inaccuracy of the model obtained with this technique.

Fig. 6.5 shows a comparison between the experimental results and the results obtained with the model proposed in chapter 3 of the step response of the DLT at different switching frequencies. A clear dependence of the dynamics of the converter with the switching frequency is noticed. Moreover, a lesser settling time is obtained for higher frequency values as well as the output voltage is greater with a higher frequency. Table 6.1 shows the numeric results for Fig. 6.5 of a performance index calculated as follows

$$FIT = 100\left(1 - \frac{\|\check{y} - y\|}{\|y - \bar{y}\|}\right)\% \tag{6.1}$$

where $\|*\|$ represents the norm of the argument, $\check{y}$ the results obtained with the theoretical model, y the experimental measurements and $\bar{y}$ the average of

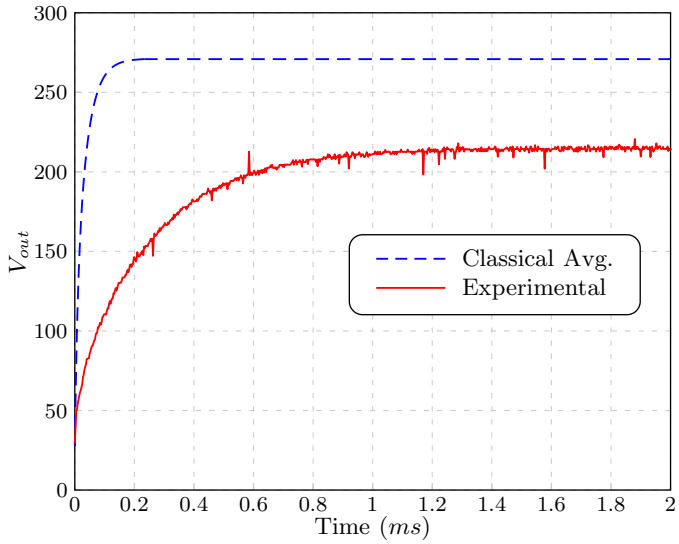


Figure 6.4: Comparison of the experimental and theoretical response V_{out}/V_{in} using the classical average model to a $31V$ step of the DLT with a resistive load $R_{load} = 2.1k\Omega$

the vector y.

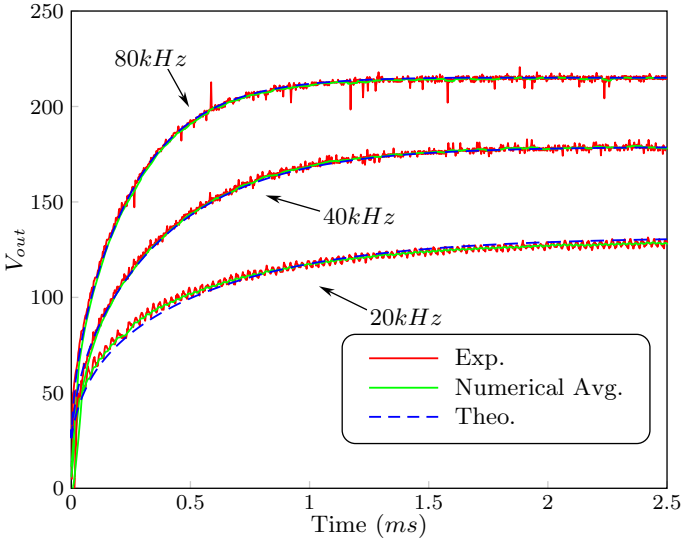


Figure 6.5: Comparison of the experimental and theoretical response V_{out}/V_{in} using the general equivalent continuous model to a $31V$ step of the DLT with a resistive load $R_{load} = 2.1k\Omega$

Fig. 6.6 shows the comparison of the incremental step response from f_{DLT} (input) to V_{out} (output) of the analytical model and the experimental results for different operating frequencies. Again, the results obtained with the theoretical

Table 6.1: FIT index for the step response V_{out}/V_{in} of Fig. 6.5

	$80kHz$	$40kHz$	$20kHz$
FIT	97%	94%	89%

model are consistent with the experimental results for the tested cases. The numerical results of the FIT indexes are shown in Table 6.2

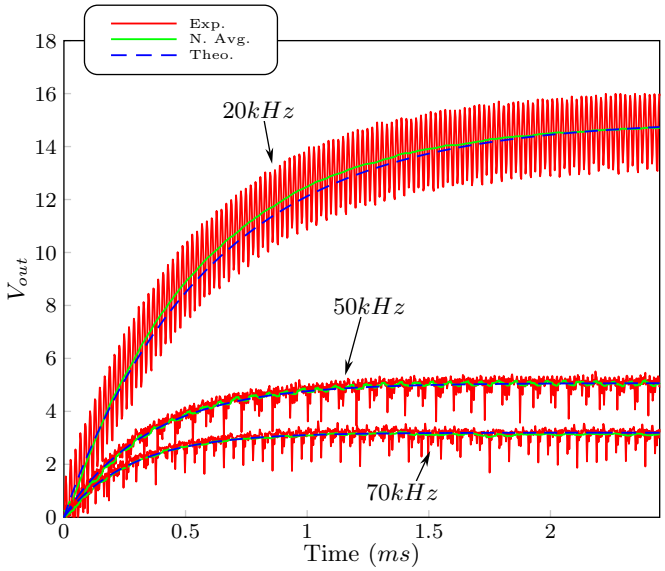


Figure 6.6: Comparison of the experimental and theoretical response (incremental) V_{out}/f_{DLT} using the general equivalent continuous model to a $31V$ step of the DLT with a resistive load $R_{load} = 2.1k\Omega$

Table 6.2: FIT index for the step response V_{out}/f_{DLT} of Fig. 6.6

	$70kHz$	$50kHz$	$20kHz$
FIT	91%	94%	94%

Fig. 6.7 shows a comparison the DC gain of the DLT as a function of switching frequency, it can be seen how the converter gain V_{out}/V_{in} increases with the frequency. Moreover, the experimental and theoretical results are consistent. The numerical result of the FIT index is shown in Table 6.3

Table 6.3: FIT index for the DC gain v.s. frequency of Fig. 6.7

	DC Gain
FIT	95%

The FIT index shows in all the cases a clear accuracy of the analytical modeling technique compared to the experimental results. Therefore, it can be used in order to design a control law.

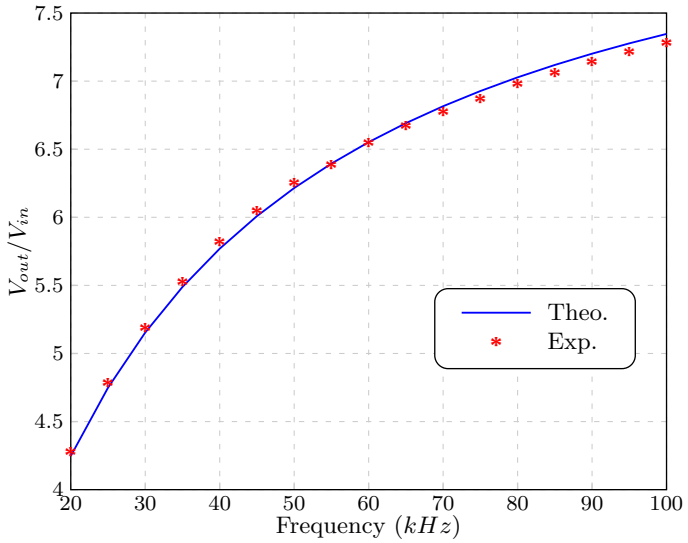


Figure 6.7: Comparison of the experimental and theoretical DC gain V_{out}/V_{in} of DLT using the general equivalent continuous model with a resistive load $R_{load} = 2.1k\Omega$

Glow discharge

Fig. 6.8 shows the glow discharge voltage as a function of the current, it can be seen that for currents less than $50mA$ the voltage varies with the current as a negative resistance. However, for currents more than $50mA$ the discharge voltage remains steady. Moreover, the discharge voltage depends on the breakdown voltage V_{BD} between the electrodes, which also depends on the distance. The possible variations on the discharge voltage are taken as perturbations in order to design the control law.

6.4.2 Controller

One objective of the control law is to be able to start-up the discharge and maintain its current to a certain value. Fig. 6.9 shows the discharge start-up by the controller with a current set point of $50mA$. The discharge begins when the voltage between the electrodes V_{gd} reach $3000V$ approximately. At this instant the voltage between the electrodes falls immediately to a voltage under $250V$ and the current through the discharge i_{load} starts to raise. The controller reduce the buck-boost voltage V_{BB} and therefore the DLT voltage V_{DLT} in order to set the current to the desired level.

The step response of the controller with the glow discharge already generated is shown in Fig. 6.10. It can be seen V_{BB} and V_{DLT} raising in order to obtain the desired current. Furthermore, the discharge voltage V_{gd} falls at 0.2s while the current is rising. However this perturbation is considered in the controller design and it is rejected by this as expected. In Fig. 6.11 the response of the controller to a perturbation in the discharge voltage V_{gd} is showed resulting in a fast correction of the load current i_{load}.

The behavior of the V_{gd} voltage becomes unpredictable at higher current

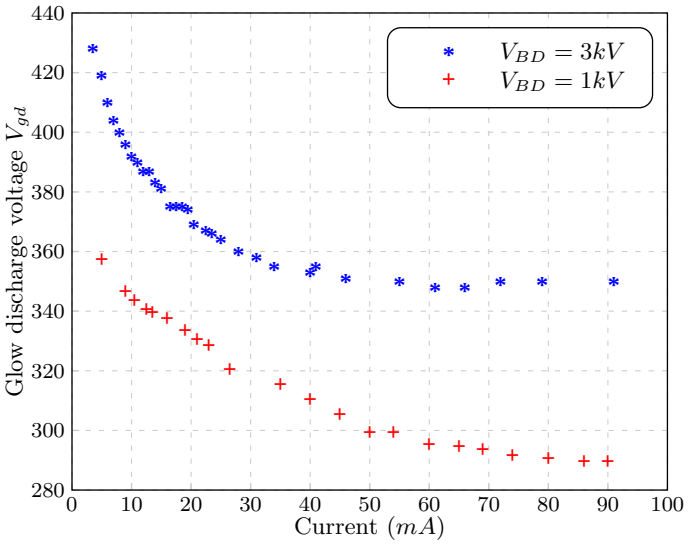


Figure 6.8: Glow discharge voltage for different breakdown voltages V_{BD} and for different current values

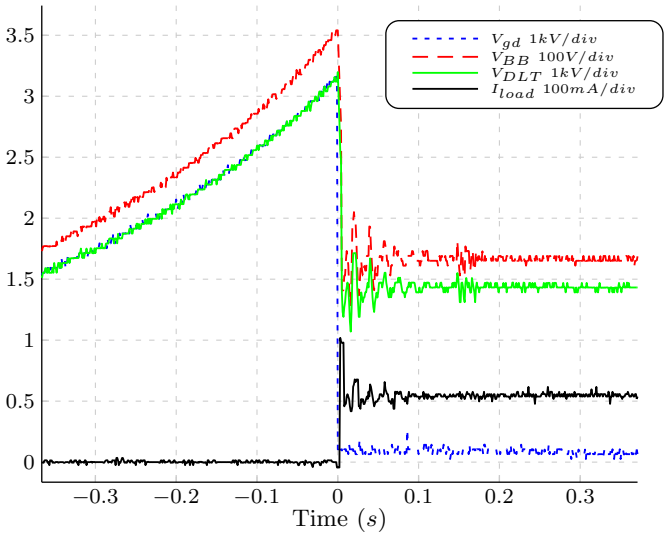


Figure 6.9: Glow discharge start-up by the controller

values. For low currents (i.e $i_{load} = 20mA$) the discharge voltage remains constant. However, for higher current values (i.e $i_{load} = 75mA$) the discharge voltage varies in the time with a constant current set point as shown in Fig. 6.12. Since these perturbations are taken into account in the controller design their effects on the load current i_{load} are reduced.

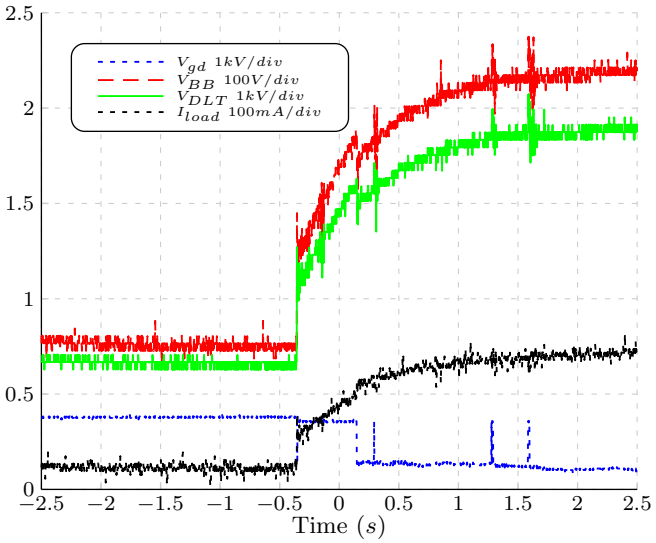


Figure 6.10: Controller step response from $i_{load} = 10A$ to $i_{load} = 70mA$ at $t = -0.4s$

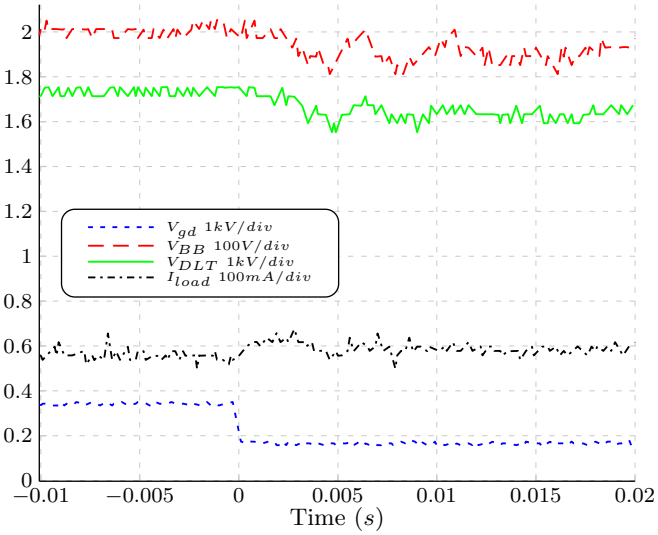


Figure 6.11: Step response to a perturbation in the discharge voltage V_{gd}

6.5 Conclusions

A DLT converter was successfully implemented with a $3000V$ $100mA$ output for a glow discharge application. Moreover, the poor accuracy of the classical average modeling technique is demonstrated and its effects on the controllers are evaluated. A new modeling technique proposed in chapter 3 is evaluated and validated with experimental measurements, this technique showed a great accuracy measured with FIT index. Moreover, the effects of the switching frequency

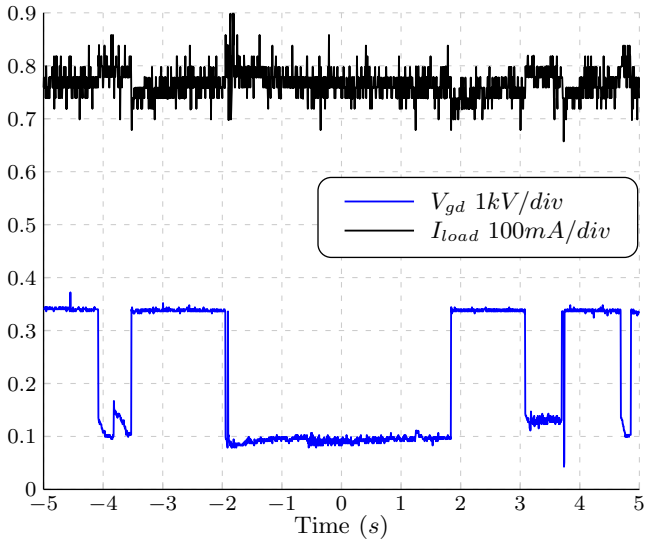


Figure 6.12: Glow discharge voltage behavior at $i_{load} = 75mA$

on the converter response are evaluated showing a strong dependence.

Since the output voltage of DLT is differential and not referenced to a common point, the measurement of the output current is performed with a high voltage insulated hall sensor.

Due to the principle of functionality of the multilevel converter, abrupt changes on its input voltage generates very high current spikes through the DLT switches. Therefore, the controller speed was limited to avoid over-current on the switches. The use of the duty cycle of the DLT d_{DLT} as a control signal was evaluated. However, for the particular values of R_C and R_S used of the implementation this duty cycle has minimum effect on the output voltage and current. Finally, the performance of a $\mu(DK)$ controller is tested on the discharge start-up successfully.

In order to reduce the current spikes produced by abrupt voltage changes, small inductances could be added in series to the capacitors of DLT.

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