IMPLEMENTACIÓN DE UN SISTEMA DE COMPENSACIÓN DE REACTIVOS

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TRABAJO DE GRADO DE PROFUNDIZACIÓN DE MAESTRÍA PARA OPTAR POR EL TITULO DE MAGISTER EN INGENIERÍA ELECTRÓNICA

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"La universidad no se hace responsable de los conceptos emitidos por sus alumnos en sus proyectos de grado.

Sólo velará porque no se duplique nada contrario al dogma y la moral católica y porque los trabajos no contengan ataques o polémicas puramente personales. Antes bien, que se vea en ellos el anhelo de buscar la verdad y la justicia".

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GLOSSARY

HB: H-Bridge
CEMI: Cascade Equal Multilevel Inverter
QLMI: Quasi-Linear Multilevel Inverter
BHMI: Binary Hybrid Multilevel Inverter
THMI: Trinary Hybrid Multilevel Inverter
DC: Direct Voltage
AC: Alternative voltage
DSP: Digital Signal Processor

1 Introduction:

Nowadays renewable energies are very popular around the world. One that is commonly used is the solar photovoltaic energy, which converts the light energy radiated by the sun into electrical energy, by means of an array of photovoltaic cells.

In faraway places the solar energy is generated to be used in an isolated mode. This means that energy storage is necessary to cover the differences between the instantaneous demanded and produced power.

In cities or big towns the solar energy is used in a grid tie mode, supplying current to the local network while the grid is working properly.

The energy produced by this array can be considered as a DC power supply. In consequence this energy needs to be converted to AC voltage for its use in standard power appliances.

Due to the needs to convert DC voltage to AC voltage, a lot of persons are working designing and studying different kinds of inverters, improving efficiency and robustness working in isolated or grid tie mode.

About the inverter in grid tie mode, these inverters can work supplying current in phase or with any phase shift. This function is called reactive power compensator. This helps to improve the Displacement Power Factor of the load in the vicinity of the inverter.

Nowadays the inverters have one or more levels. The inverters of one level needs inductors with high inductance and able to support high current, in the other hand the commons multilevel inverters are flying capacitors inverter and clamped diode inverter. Flying capacitor inverter with high number of level the control of charge and discharge of the capacitor is very complicated. In Clamped diode inverter, with high number of levels needs a lot of diodes and produce an imbalance on the DC links made by capacitors, and the inverter would be very complex to implement and control [1].

Due to these disadvantages of the commons PWM and multilevel inverters this project seeks a novel topology of a inverter to solves the disadvantages of the inverters mentioned previously.

The objective of this project is to design, simulate and implement an inverter topology to supply current to the local network. This current could be in phase, lagging or leading to the grid voltage.

The first part of the project is the study of several topologies of multilevel inverters, selecting the Trinary Hybrid Multilevel Inverter as the best choice. This is a novel multilevel inverter that has the most number of levels per H-Bridge. Then this topology is modeled and simulated in open loop, in order to verify the model and proceed with the design and simulation of a linear control and a nonlinear control. The nonlinear control is designed with Sliding mode control technique using a novel nonlinear function. Finally, the implementation of the hardware and both controls are made, in order to validate the theory. Also comparative analysis between the nonlinear control and linear control are done evaluating performance, efficiency and robustness.

The block diagram of the project is shown in Figure 1-1.

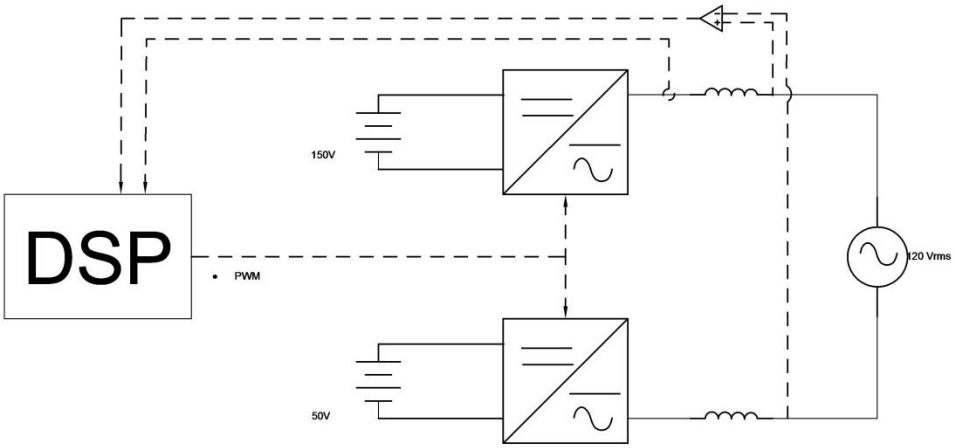

Figure 1-1 Block diagram of the thesis

1.1 Objectives

1.1.1 General Objectives:

- Design an Inverter of 200 VA at 120 Vrms of output and a total input of 200 V able to supply current to the local network on phase, lagging, or leading to reduce the electricity consumption from the local network and improve the displacement power factor.

1.1.2 Specific Objectives

- Implement a novel topology of an inverter of 200 VA at 120 Vrms of output and a total input of 200 V of input in open loop with a resistive load.
- Design and simulate one linear control and one nonlinear control to the inverter in grid tie mode and evaluate performance, transient response and disturbance response.
- Validate the two controls designed in the inverter implemented in grid tie mode and analyze and compare performance (robustness, transient response and disturbance response).

2 Theoretical Framework

This Theoretical framework deals with the previous work about H bridge multilevel inverter. It begins explaining the different kinds of multilevel H bridge inverters and then explains the different modulation strategies of this kind of inverters. This part also talks about linear and nonlinear control specially sliding mode control on inverters.

2.1 H bridge multilevel Inverter:

H-Bridge multilevel Inverter is an array of H-bridges with a different isolate DC bus in each H-Bridge. Depending of the DC voltage of each H-Bridge, the Multilevel Inverter known as Cascade Multilevel Inverter, Quasi-Linear Multilevel Inverter, Binary Multilevel Inverter, or Trinary Multilevel Inverter [2]. **Figure 2-1** H-Bridge Multilevel Inverter shows the general topology of the H-Bridge Multilevel Inverter.

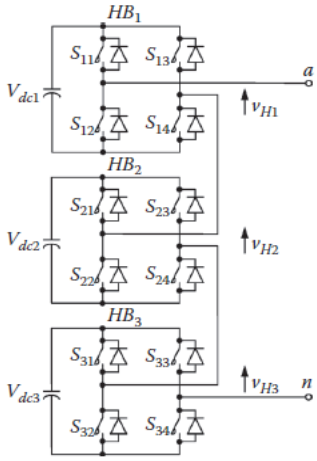

Figure 2-1 H-Bridge Multilevel Inverter

Where HB_i is the *i*-th H-Bridge, $V_{dc_i}$is the power supply of the $HB_i$and V_{H_i} is the output voltage of HB_i.

2.1.1 Cascaded Equal Voltage Multilevel Inverter (CEMI):

In a CEMI all DC links are the same.

$$V_{dc_1} = V_{dc_2} = .. = V_{dc_i} = V_{dc_{i+1}} = V_{dc_h} = E \qquad \text{Eq. 2-1}$$

Where *E* is the voltage of the first H-Bridge, that in CEMI is the same of the other H-Bridge.

In this case a CEMI of h H-Bridges generate $2h + 1$ $Levels$ and has maximum amplitude of hE. The **Figure 2-2** Waveform of CEMI of 3 H-Bridge shows the waveform of a CEMI of 3 H-Bridges.

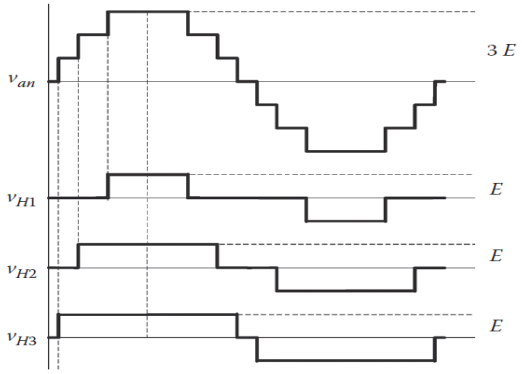

Figure 2-2 Waveform of CEMI of 3 H-Bridge

2.1.2 Quasi-Linear Multilevel Inverter (QLMI):

In the QLMI the *i*-th DC link can be expressed as:

$$V_{dc_i} = \begin{cases} E\,; i = 1 \\ 2 * 3^{i-2} E\,; i \geq 2 \end{cases} \quad \text{Eq. 2-2}$$

In this case a QLMI of n H bridge has a $2\left(3^{h-1}\right) + 1$ $Levels$ and has a maximum amplitude of 3^{h-1} E . The **Figure 2-3** shows the waveform of QLMI of 3 H-Bridges.

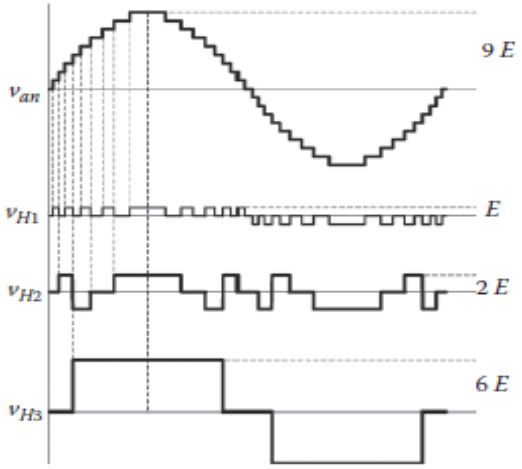

Figure 2-3 Waveform of QLMI of 3 H-Bridge

2.1.3 Binary Hybrid Multilevel Inverter (BHMI):

In the BHMI the *i*-th DC link is double of the (*i-1)*-th H bridge DC link.

$$Vdc_1 = E, V_{dc_2} = 2E, V_{dc_3} = 4E \ldots V_{dc_i} = 2^{i-1}E \quad \text{Eq. 2-3}$$

In this case an BHMI of h H-Bridge has a $2^{n+1}-1\ Levels$ and has a maximum amplitude of $(2^n-1)E$. The **Figure 2-4** shows the waveform of BHMI 3 H-Bridges.

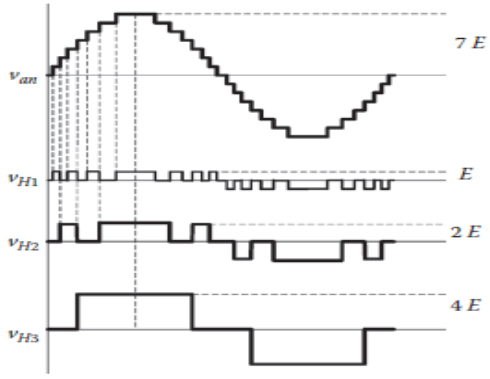

Figure 2-4 Waveform of a BHMI of 3 H-Bridge

2.1.4 Trinary Hybrid Multilevel Inverter (THMI):

In the THMI the *i*-th DC link is three times of the (*i-1)*-th H bridge DC link.

$$Vdc_1 = E, V_{dc_2} = 3E, V_{dc_3} = 9E \ldots V_{dc_i} = 3^{i-1}E \qquad \text{Eq. 2-4}$$

In this case an THMI of h H-Bridge has a $3^h Levels$ and has a maximum amplitude of $\frac{(3^h-1)}{2}E$. The **Figure 2-5** shows the waveform of a THMI of 3 H-Bridges.

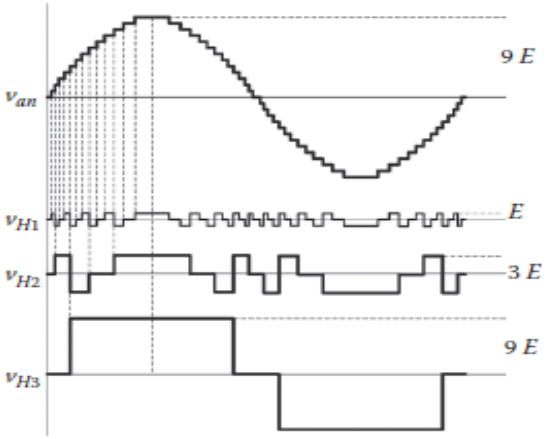

Figure 2-5 Waveform of a THMI of 3 H-Bridge

2.1.5 Comparative Analysis of the different topologies:

This is a comparative analysis of each Multilevel Inverter of h H-Bridges

Multilevel Inverter	levels	Maximum amplitude
CEMI	$2h+1$	hE
QLMI	$2*\left(3^{h-2}\right)+1$	$3^{h-1}E$
BHMI	$2^{n+1}-1$	$(2^h-1)E$
THMI	3^h	$\frac{3^h-1}{2}E$

Table 2.1 Comparative analysis of multilevel H-Bridge Inverters

Table 2.1 shows that the maximum number of levels is THMI. Thus, this converter is considered the best choice.

Because THMI has the highest number of levels, this presents the less THD among the alternative of Table 2.1.

2.2 Switching function of THMI

Suppose a THMI of h H-Bridge where v_{an} is the output voltage.

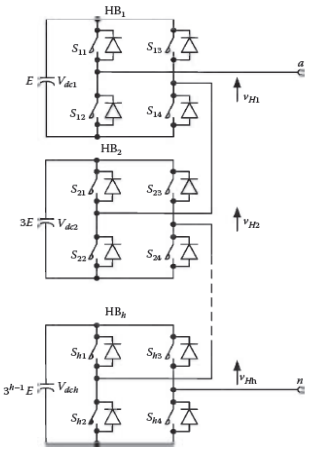

Figure 2-6 THMI Topology

According Figure 2-6 THMI Topology the output voltage VH_i is:

$$VH_i = F_i V_{dc_i} \quad \text{Eq. 2-5}$$

Where F_i is a function modulation of the *i*-th H-Bridge. This defines the position of the switching device and it is defined as: Eq. 2-6

$$F_i = \begin{cases} -1; & S_1 \equiv S_4 \equiv 0 \ \wedge \ S_2 \equiv S_3 \equiv 1 \\ 0; & S_1 \equiv S_3 \equiv \overline{S_2} \equiv \overline{S_4} \\ 1; & S_1 \equiv S_4 \equiv 1 \ \wedge \ S_2 \equiv S_3 \equiv 0 \end{cases}$$

The output voltage of each H-Bridge VH_i is:

$$VH_i = 3^{i-1} F_i E \quad \text{Eq. 2-7}$$

The total output voltage v_{an} [1] is:

$$v_{an} = \sum_{i=1}^{h} VH_i \quad \text{Eq. 2-8}$$

$$v_{an} = E \sum_{i=1}^{h} 3^{i-1} F_i \quad \text{Eq. 2-9}$$

In order to obtain a $v_{an} = l * E$, l must be an integer defined as:

$$-\frac{(3^h - 1)}{2} < l < \frac{(3^h - 1)}{2} \quad \text{Eq. 2-10}$$

$$v_{an} = lE = E \sum_{i=1}^{h} 3^{i-1} F_i \quad \text{Eq. 2-11}$$

$$l = \sum_{i=1}^{h} 3^{i-1} F_i \quad \text{Eq. 2-12}$$

F function is defined as:

$$\begin{aligned}
&F_h = sign(l) * sign\left(|l| - \frac{3^{h-1} - 1}{2}\right) \\
&F_{h-1} = sign(l) * sign\left(|l| - 3^{h-1}|F_h| - \frac{3^{h-2} - 1}{2}\right) \\
&\dots \\
&F_i = sign(l) * sign\left(|l| - \sum_{k=i+1}^{h} (3^{k-1}|F_k|) - \frac{3^{i-1} - 1}{2}\right) \\
&\dots \\
&F_2 = sign(l) * sign\left(|l| - \sum_{k=3}^{h} (3^{k-1}|F_k|) - 1\right) \\
&F_1 = sign(l) * sign\left(|l| - \sum_{k=2}^{h} (3^{k-1}|F_k|)\right)
\end{aligned} \quad \text{Eq. 2-13}$$

2.3 Modulation Strategies of THMI:

This chapter explains the modulation strategies to THMI. The modulation strategies can be at low frequency or at high frequency, and seeks the harmonic elimination.

2.3.1 Step Modulation

The objective of step modulation is to build a symmetrical quarter wave eliminating harmonics switching at a certain angle from one level to other.

Consider ζ the number of angles in the first quarter-wave and σ the numbers of positives levels.

In a step modulation ζ= σ, because the switching is only to the immediately higher level. The step modulation can eliminate a limited number of harmonics depending on the number of possible levels.

Applying Fourier analysis to the odds harmonics (even harmonics are 0) the *j*-th harmonic can be expressed as:

$$|v_{an}|_j = \frac{4}{j\pi}\sum_{i=1}^{\sigma}\left(Ecos(j\theta_i)\right) \quad \text{Eq. 2-14}$$

Where $|v_{an}|_j$ is the component of the *j*-th harmonic of the output voltage.

And θ_i is the switching angle that switchs from (*i-1)*-th level to *i*-th level.

And consider MR the relative modulation index and is expressed as:

$$MR = \frac{\pi|v_{an}|_1}{4\sigma E} \quad \text{Eq. 2-15}$$

We can obtain the next system of nonlinear equation:

$$\begin{aligned} &\cos(\theta_1) + \cos(\theta_2) \dots \cos(\theta_\sigma) = \sigma MR \\ &\cos(3\theta_1) + \cos(3\theta_2) \dots \cos(3\theta_\sigma) = 0 \\ &\cos(5\theta_1) + \cos(5\theta_2) \dots \cos(5\theta_\sigma) = 0 \end{aligned} \quad \text{Eq. 2-166}$$

$$\dots$$
$$\cos\left((2\sigma-1)\theta_1\right) + \cos((2\sigma-1)\theta_2) \dots \cos\left((2\sigma-1)\theta_\sigma\right) = 0$$

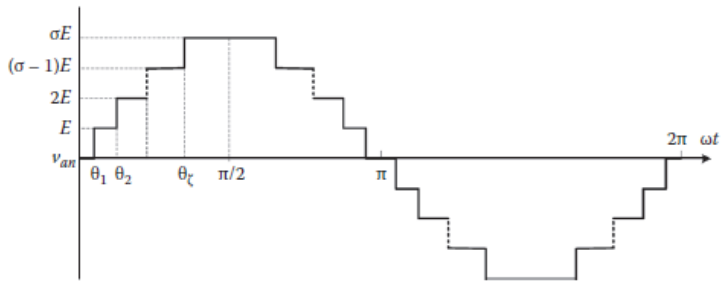

Figure 2-7 Step Modulation Waveform

Figure 2-7 shows the Waveform of a THMI with a step modulation strategy.

2.3.2 Virtual Stage Modulation:

The virtual stage modulation is another low frequency strategy like step modulation with the difference that it can pass to a higher or lower level in the same quarter –wave if it would be necessary, considering this condition in a virtual stage modulation the number of switching angle ζ is more than the positives levels σ.

$$\sum_{i=1}^{\alpha}\cos(\theta_{pi}) - \sum_{i=1}^{\beta}\cos(\theta_{ni}) = \sigma MR$$
$$\sum_{i=1}^{\alpha}\cos(3\theta_{pi}) - \sum_{i=1}^{\beta}\cos(3\theta_{ni}) = 0$$
$$\sum_{i=1}^{\alpha}\cos(5\theta_{pi}) - \sum_{i=1}^{\beta}\cos(5\theta_{ni}) = 0 \qquad \text{Eq. 2-17}$$
$$\ldots$$
$$\sum_{i=1}^{\alpha}\cos\left((2\sigma-1)\theta_{pi}\right) - \sum_{i=1}^{\beta}\cos((2\sigma-1)\theta_{ni}) = 0$$

Where θ_{pi} is the *i*-th angle that switches to a higher level and θ_{ni} is the *i*-th angle that switches to a lower level, and α is the number of switching to higher and β are the number of switching to lower.

Figure 2-8 Virtual stage modulation shows the Virtual Stage Modulation.

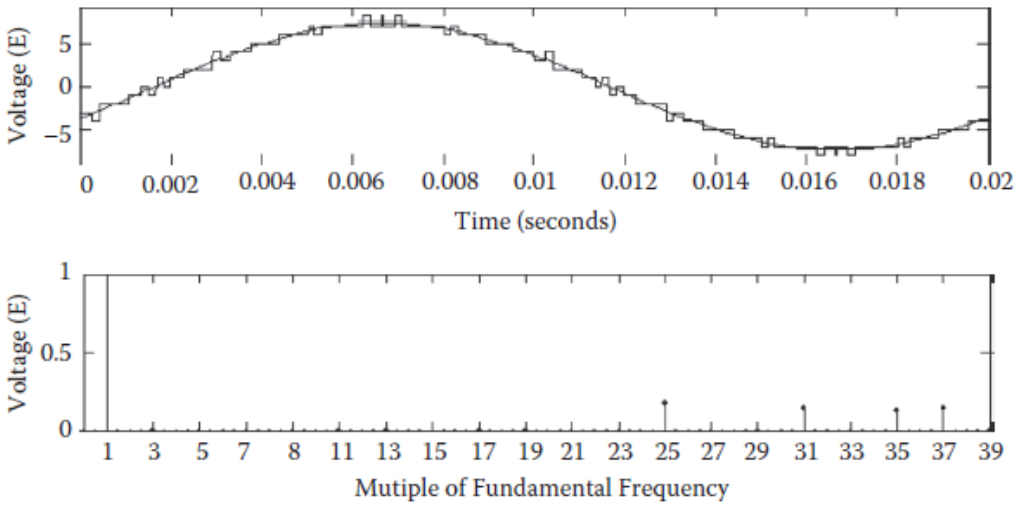

Figure 2-8 Virtual stage modulation

2.3.3 Hybrid Modulation:

The Hybrid modulation strategy is a mixed technique where the higher Power H-Bridge switch at step modulation and the lower-power H-Bridge switch at High frequency PWM

2.3.4 Sub-Harmonic PWM Modulation:

A Sub-Harmonic modulation is a high frequency PWM technique with the difference that in this case it used l-1 carrier triangles wave.

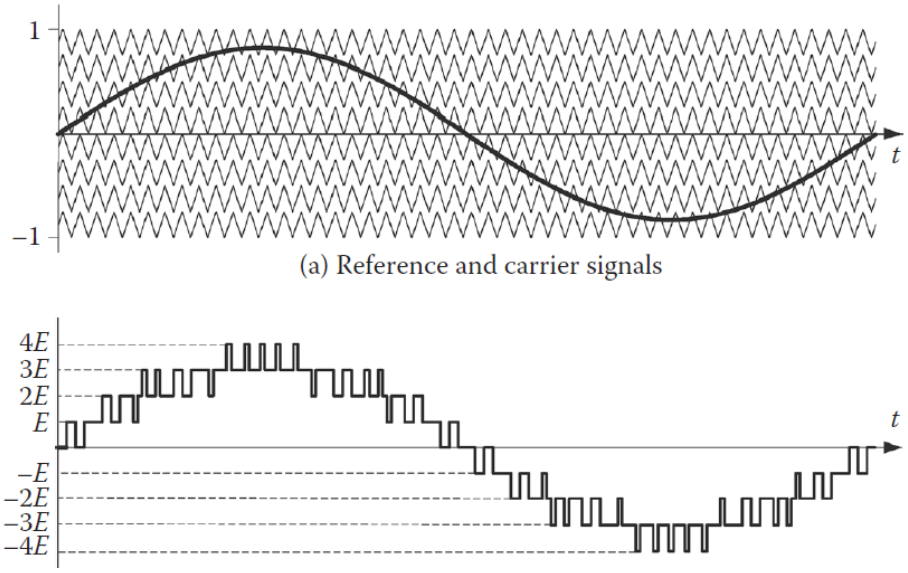

Figure 2-9 Sub-Harmonic PWM Modulation

2.3.5 Comparative analysis of the different modulation strategies:

Modulation strategy	Advantages	Disadvantages
Step Modulation	1. The inverter Switches at Low frequency produces low switching losses	1. Limited number of harmonics eliminated 2. Complicated math operations to the processor
Virtual Stage Modulation	1. The inverter switches at Low frequency produces low switching losses 2. Unlimited number of harmonics eliminated	3. The complexity of math operations increase as the number of harmonics to be eliminated
Hybrid modulation	1. The higher voltage H-Bridges switches at low frequency and produces low switching losses. 2. The lower voltage H-Bridges switches at high frequency eliminating the high order harmonics	1. Calculate the switching angle of the higher voltage H-Bridge needs a lots resource of the processor. 2. Switching at high frequency the lower voltage H-Bridge produce high switching losses.

Sub-Harmonic PWM modulation	1. Inverter switches at higher frequency eliminating much harmonics compared to others techniques. 2. Due to THMI topology can produce a high number of levels per H-Bridge; the switching losses are less than the other topologies with this modulation. 3. The math model is easier than the low frequency modulation strategies	4. Switching at high frequency produce high switching losses.

Table 2.2 Comparative analysis of modulation strategies.

Table 2.2 shows the characteristics of each modulation strategy and infers that the Sub-Harmonic PWM modulation is the best choice because it is easy to implement in a DSP, eliminate high harmonics and in THMI the switching losses is not higher.

2.4 Linear Controller:

One of the objectives of the Project is to compare a linear controller and a nonlinear controller in the inverter .

2.4.1 PI Controller:

The Proportional-Integral (PI) controller is described in Figure 2-10

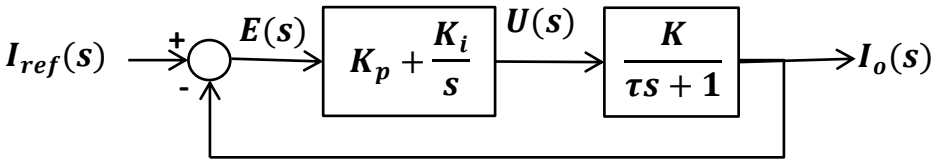

Figure 2-10 PI controller Block Diagram

Solving the block diagram in Figure 2-10 PI controller Block Diagram

$$I_{ref}(s) - I_o(s) = E(s)$$

$$E(s) = \frac{\left(\frac{K_i}{s} + K_p\right) K}{\tau s + 1}$$

$$I_o(s) = \frac{\frac{K_i K + K_p K s}{s(\tau s + 1)}}{\frac{K_i K + K_p K s}{s(\tau s + 1)} + 1}$$

$$I_o(s) = \frac{K_p K s + K_i K}{\tau s^2 + s(K_p K + 1) + K_i K}$$

$$I_o(s) = \frac{K_p}{K_i}\left(s + \frac{K_i}{K_p}\right)\left(\frac{\frac{K_i K}{\tau}}{s^2 + \frac{K_p K + 1}{\tau} s + \frac{K_i K}{\tau}}\right) \quad \text{Eq. 2-18}$$

Eq. 2-18 describes the close loop transfer function with a PI controller. In the PI controller the transfer function is defined by a gain, a real zero and a pair of complex pole or two real poles depending the values on K_p and K_i. [3]

2.5 Nonlinear Control

2.5.1 Lyapunov Function

Suppose a nonlinear system defined as **Eq. 2-19** where the equilibrium point is X=0, and suppose a Function V(X).[4]

$$\dot{\boldsymbol{X}} = \boldsymbol{F}(\boldsymbol{X}, \boldsymbol{U}) \quad \text{Eq. 2-19}$$

V(X) is a Lyapunov function if:

$$V(X) > 0\,; X \neq 0$$
$$V(X) = 0; X = 0$$
$$\dot{V}(X) \leq 0$$

If exist a Lyapunov Function the system is stable.

2.5.2 Sliding Mode Control

Suppose a Surface S function of the states of **Eq. 2-19**

$$S = \{X \in R^n | S(X) = 0\} \quad \text{Eq. 2-20}$$

Now suppose a Lyapunov Function of the surface defined in **Eq. 2-20**

$$V(S) = \frac{1}{2} S^2 \quad \text{Eq. 2-21}$$
$$\dot{V}(S) = S\dot{S}$$
$$\dot{V}(S) = S \frac{\partial S}{\partial X}^T F(X, U)$$

The objective of the technique is to find an input U(t) to ensure that V(S) is a Lyapunov Function.[5]–[8]

3 Specifications:

This chapter defines how many H-Bridges is going to have the inverter, the DC voltage of each H-Bridge, the switching devices of each H-Bridge and the dead time of the switching devices.

3.1 Inputs/Outputs:

The inverter must have a total power supply inputs of 200 V, and an output of 120 Vrms tied to the grid. The inverter has to be able to supply 200 VA

3.2 Structure of the system:

In the **Table 2.1** it can be inferred that the best multilevel converter is THMI because is the inverter that produce the most number of levels per H-Bridge.

Table 2.2 describes all the modulation strategies and the result is that Sub-Harmonic PWM modulation is the best choice for a THMI inverter because the switching losses is not too high, it is easy to model and does not need a lot of computational resources.

Once the topology and the modulation strategy are defined, it is necessary to define the quantity of H-Bridges that is going to have the inverter. Considering the total input voltage is 200 V and according **Figure 2-6** THMI Topology the value of the smallest power supply is E. E can be defined as E = 200 / h where h is the number of H-Bridges. The Lowest power supply will be 50 V because at this value we can find MOSFETs fast enough and with the enough current capacity for a 200 VA inverter.

If the lowest H-Bridge (LV) is supplied at 50 V, according the THMI topology the highest H-Bridge must be supplied at 150 V (HV).

Because the sources may supply positive currents at any time, it is necessary input filters in each H-Bridge.

Considering all of these issues, the structure of the system is the one shown in **Figure 3-1** System Structure

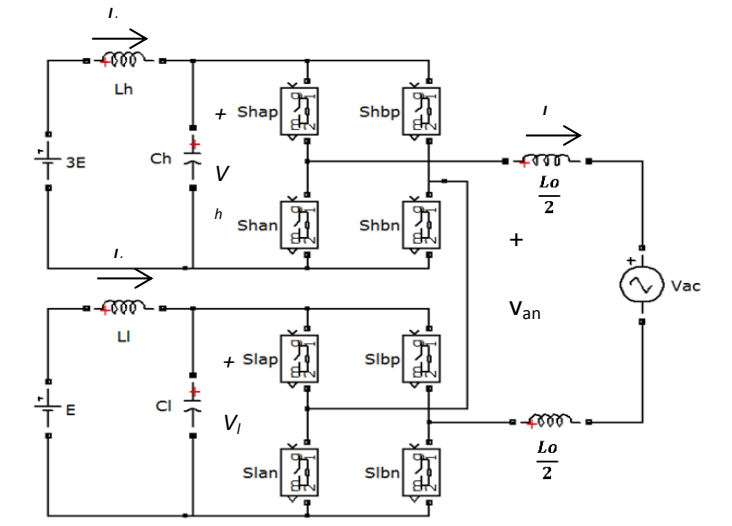

Figure 3-1 System Structure

Where L_h, C_h are the inductor and the capacitor respectively of the input filter of the higher H-Bridge. L_l , C_l are the inductor and the capacitor respectively of the input filter of the lower H-BridgeL_o is the output inductors. I_h , I_l , I_o are the currents through L_h, L_l, L_o respectively . V_h, V_l are the voltages in C_h and C_l respectively. V_{ac} is the voltage in the local network.

4 Design and Simulations

4.1 Design of gate signals:

Considering the F function in **Eq. 2-6** for the switching device of THMI of 2 H-Bridges shown in **Figure 3-1** System Structure is described in **Eq. 4-1**

$$F_h = \begin{cases} 1; & S_{hap} \equiv S_{hbn} \equiv 1 \wedge S_{han} \equiv S_{hbp} \equiv 0 \\ 0; & S_{hap} \equiv S_{hbp} \equiv \overline{S_{han}} \equiv \overline{S_{hbn}} \\ -1 & S_{hap} \equiv S_{hbn} \equiv 0 \wedge S_{han} \equiv S_{hbp} \equiv 1 \end{cases} \quad \text{Eq. 4-1}$$

Where 1 represent the switch in ON state, and 0 represent the switch in OFF state.

The gate signals to obtain a specific level l is defined replacing **Eq. 2-13** in **Eq. 4-2**

$$F_2 = sgn(l) * sgn(|l| - 1) \quad \text{Eq. 4-2}$$

$$F_1 = sgn(l) * sgn(|l| - 3|F_2|)$$

Where l is an integer between [-4, 4] and represents the level of the inverter at this moment.

In the PWM modulation the signal is a continuous reference between [-4, 4], because 4 is the highest value of the reference and -4 the lowest.

$Vref$ is divided in 8 intervals, [-4,-3]; [-3,-2];[-2,-1];[-1,0];[0,1];[1,2];[2,3];[3,4] and is shown in **Figure 4-1.**

8 carrier signals are generated, one for each interval, and compared with each sliced of V_{ref}.

Then the results of the PWM for each piece are added, and the result of the sum is the $l(t)$, which is an integer between [-4, 4]. This will be the input to obtain F_2 and F_1.

The block diagram in **Figure 4-2** Block Diagram to obtain l(t) describes this process to obtain $l(t)$, on the top of left part describes the process to divide V_{ref} , on the top of right part describes the generation of the 8 carrier signals, and in the bottom part describes the sum of each PWM modulation of each part of V_{ref}.

Figure 4-1 shows the waveform of the carrier signals and the sliced v_{ref}.

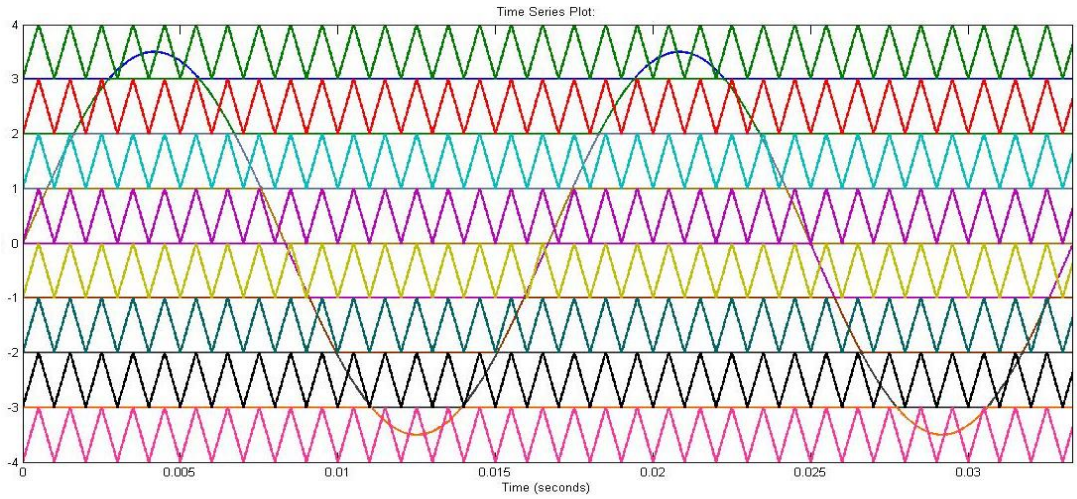

Figure 4-1 waveforms of carrier and sliced signal

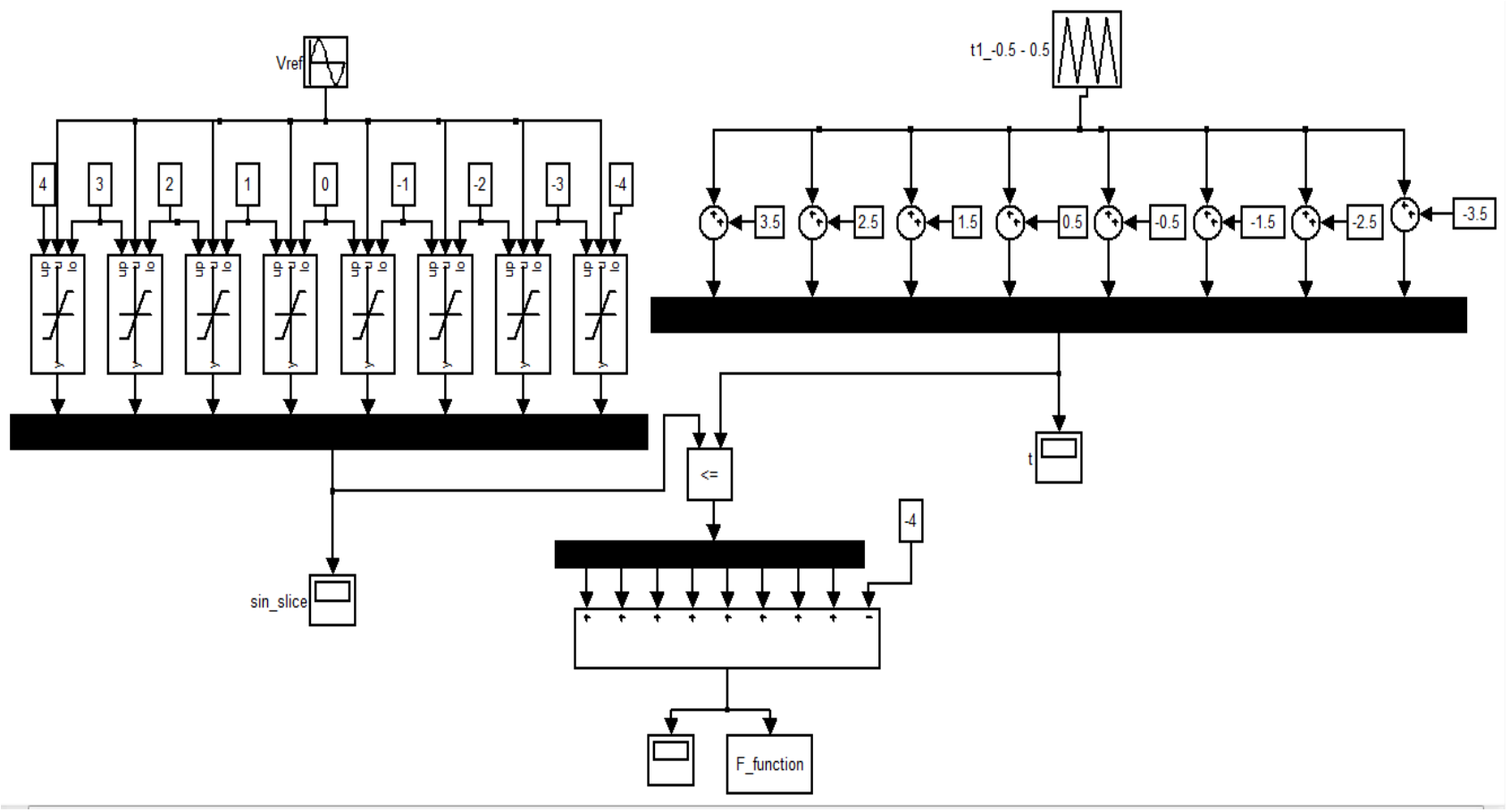

Figure 4-2 Block Diagram to obtain I(t)

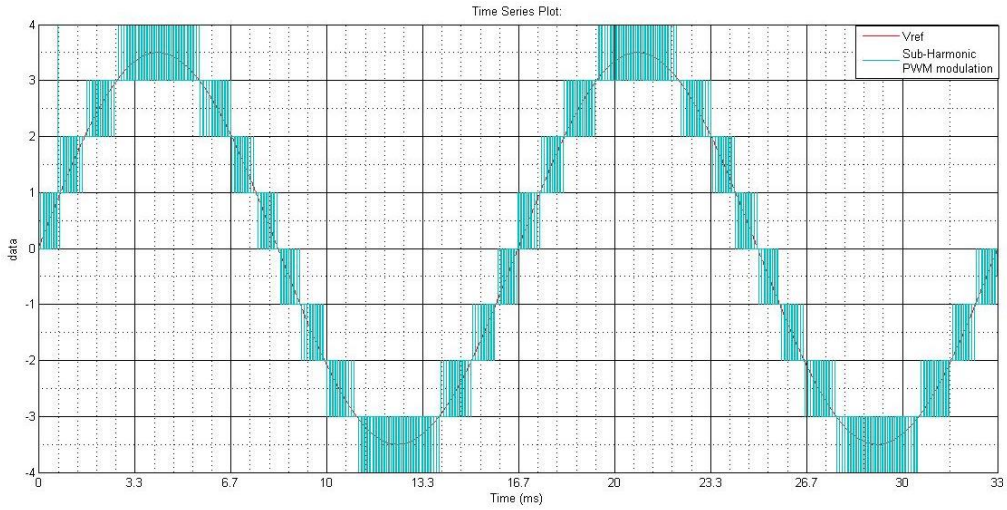

Figure 4-3 PWM Sub-Harmonic modulation

In **Figure 4-3** PWM Sub-Harmonic modulation that describes the $l(t)$ function according v_{ref}.

In order to implement a PWM in a DSP(Digital Signal Processor) with de PWM modules of the DSP, it is necessary to convert the sub-harmonic modulation into a common modulation, for this reason a look up table is generated by a F function described in **Eq. 4-3**

$$F(l) = (S_{ha}, S_{hb}, S_{la}, S_{lb}) \quad \text{Eq. 4-3}$$

$F(-4) = (0,1,0,1)$
$F(-3) = (0,1,0,0); (0,1,1,1)$
$F(-2) = (0,1,1,0)$
$F(-1) = (0,0,0,1);\ (1,1,0,1);$
$F(0) = (0,0,0,0); (0,0,1,1); (1,1,0,0); (1,1,1,1)$
$F(1) = (0,0,1,0); (1,1,1,0)$
$F(2) = (1,0,0,1)$
$F(3) = (1,0,0,0); (1,0,1,1)$
$F(4) = (1,0,1,0)$

Where $S_{ha} \equiv S_{hap} \equiv \overline{S_{han}};\ S_{hb} \equiv S_{hbp} \equiv \overline{S_{hbn}}; S_{la} \equiv S_{lap} \equiv \overline{S_{lan}};\ S_{lb} \equiv S_{lap} \equiv \overline{S_{lan}};$

It could generate many duty cycle function for $S_{ha}, S_{hb},\ S_{la}, and\ S_{lb}$

A possible duty cycle function of each switching device that satisfies **Eq. 4-3** is shown in **Figure 4-4** Duties cycles

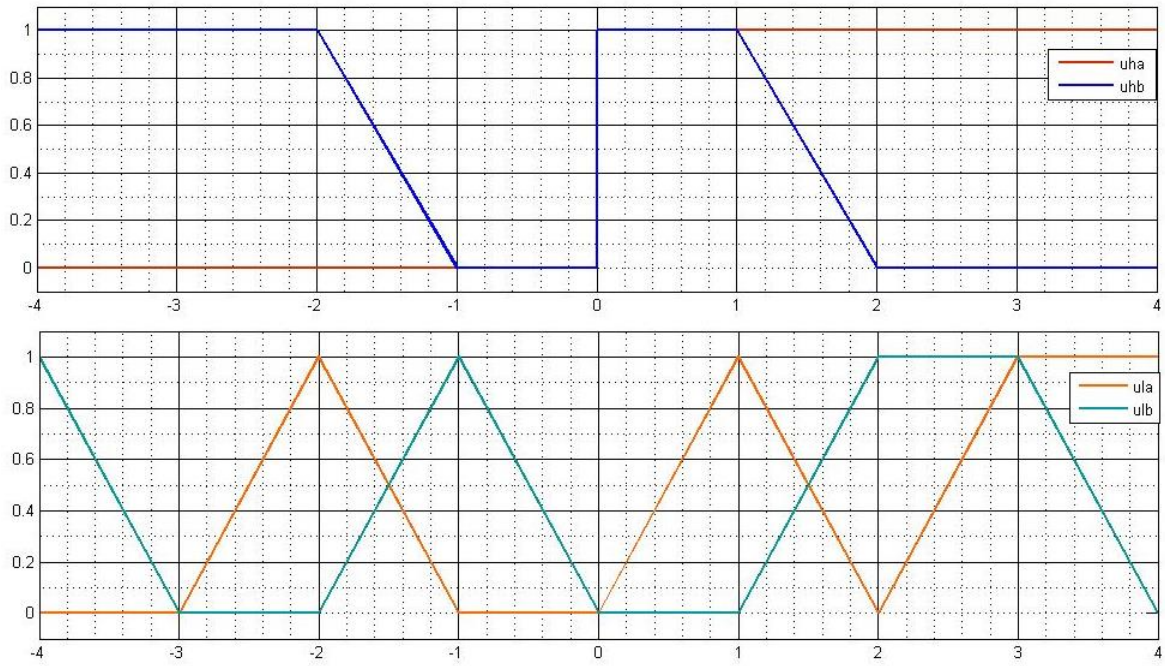

Figure 4-4 Duties cycles

Where $u_{xy} = \widehat{s_{xy}}$

The analytic function of each duty cycle is defined in Eq. 4-4

$$if(-4 < v_{ref} < -3)\ \begin{pmatrix} u_{ha} \\ u_{hb} \\ u_{la} \\ u_{lb} \end{pmatrix} = \begin{pmatrix} 0 \\ 1 \\ 0 \\ -v_{ref} - 3 \end{pmatrix} \quad if(-3 < v_{ref} < -2)\ \begin{pmatrix} u_{ha} \\ u_{hb} \\ u_{la} \\ u_{lb} \end{pmatrix} = \begin{pmatrix} 0 \\ 1 \\ 0 \\ v_{ref} + 3 \end{pmatrix}$$

$$if(-2 < v_{ref} < -1)\ \begin{pmatrix} u_{ha} \\ u_{hb} \\ u_{la} \\ u_{lb} \end{pmatrix} = \begin{pmatrix} 0 \\ -v_{ref} - 1 \\ -v_{ref} - 1 \\ v_{ref} + 2 \end{pmatrix} \quad if(-1 < v_{ref} < 0)\ \begin{pmatrix} u_{ha} \\ u_{hb} \\ u_{la} \\ u_{lb} \end{pmatrix} = \begin{pmatrix} 0 \\ 0 \\ 0 \\ -v_{ref} \end{pmatrix}$$

$$if(0 < v_{ref} < 1)\ \begin{pmatrix} u_{ha} \\ u_{hb} \\ u_{la} \\ u_{lb} \end{pmatrix} = \begin{pmatrix} 1 \\ 1 \\ v_{ref} \\ 0 \end{pmatrix} \quad if(1 < v_{ref} < 2)\ \begin{pmatrix} u_{ha} \\ u_{hb} \\ u_{la} \\ u_{lb} \end{pmatrix} = \begin{pmatrix} 1 \\ -v_{ref} + 2 \\ -v_{ref} + 2 \\ v_{ref} - 1 \end{pmatrix}$$

$$if(2 < v_{ref} < 3)\ \begin{pmatrix} u_{ha} \\ u_{hb} \\ u_{la} \\ u_{lb} \end{pmatrix} = \begin{pmatrix} 1 \\ 0 \\ v_{ref} - 2 \\ 1 \end{pmatrix} \quad if(3 < v_{ref} < 4)\ \begin{pmatrix} u_{ha} \\ u_{hb} \\ u_{la} \\ u_{lb} \end{pmatrix} = \begin{pmatrix} 1 \\ 0 \\ 1 \\ -v_{ref} + 4 \end{pmatrix}$$

Eq. 4-4

Notice in Figure 4-4 Duties cycles that $\boldsymbol{u_{la}}$ and $\boldsymbol{u_{lb}}$ when one function is constant, the other is a linear function, except between [-2, -1] and [2, 1] in this case both are linear function with different slope signs, and the Eq. 4-3 shows in this points the switching devices are the negative of the others. For this reason it is necessary to change the PWM modulation in $\boldsymbol{S_{la} or\ S_{lb}}$, inverting the carrier or changing the comparison function between the carrier and reference, then take the complement of the duty cycle.

Figure 4-5 shows a block diagram of the PWM of each input

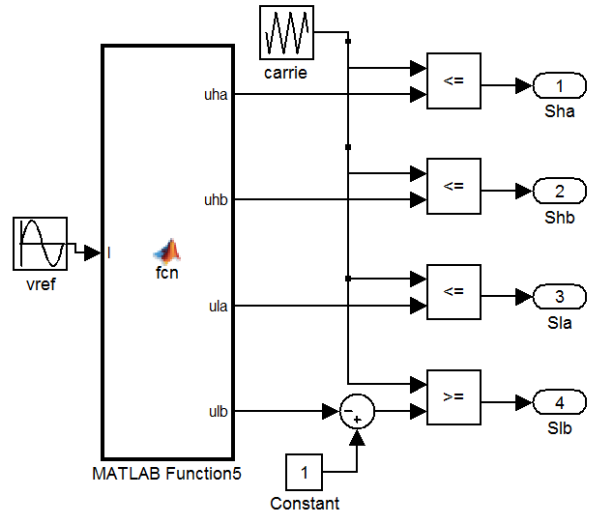

Figure 4-5 Converting into a common PWM

4.2 Design of the switching frequency and the switching devices:

In this chapter the objective is to select the switching frequency of the system and the switching devices of each H-Bridge.

The switching frequency is chosen at 100 kHz because with a period of 10µs the dead time can be 200ns, time enough for a commercial MOSFET . Due to this frequency, the switching devices of the higher H-Bridge are 4 MOSFETs IRFP350 with a V_{DS} =400V, I_{ds}=10A (at 100 ◦C), R_{ds}=0,3 Ω; T_{rise}=65ns T_{fall}= 135ns and the switching devices of the lower H-Bridge are 4 MOSFETs IRF540N with a V_{DS} =100V, I_{ds}=33A (at 100 ◦C), R_{ds}=0,044Ω; T_{rise}=46ns T_{fall}= 74ns.

Figure 4-6 output voltage without in/out filters shows the waveform of the output of the inverter without output and input filter

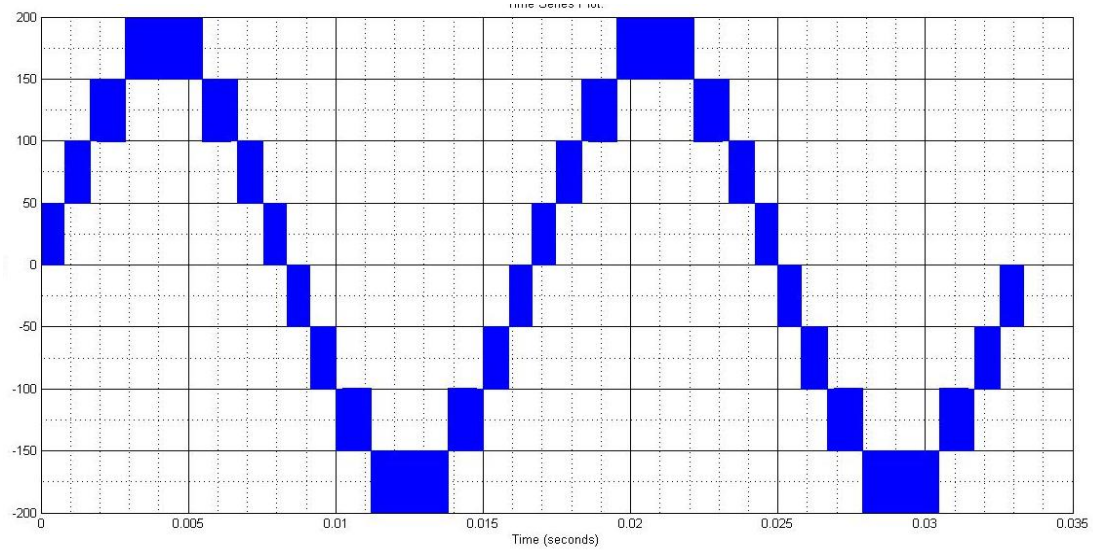

Figure 4-6 output voltage without in/out filters

4.3 Design of the output filter

Suppose that the converter is switching between a level *l* and a level *l+1*, with a *dT* subinterval in level *l+1* and *(1-d)T* subinterval in level *l*, the output v_o will be[9], [10]:

$$if\ u = l;$$
$$(lE = v_l + v_o)(1-d)T$$

$$if\ u = l+1$$
$$\big((l+1)E = v_l + v_o\big)dT$$

Taking the average of the output $\overline{v_o}$:

$$\overline{v_o} = (l+d)E$$

now to find the output inductor

$$v_l = L\frac{\Delta\, i}{\Delta\, t} = v_{an} - \overline{v_o}$$

Where v_{an} is the voltage before the inductor (switched voltage).

$$L\frac{\Delta\, i}{dT} = (l+1)E - (l+d)E$$
$$L\frac{\Delta\, i}{dT} = E(1-d)$$
$$L\,\Delta\, i = ET(d-d^2)$$
$$taking\ \ the\ worst\ value$$
$$0 = 1-2d$$
$$d = \frac{1}{2}$$

$$L\,\Delta_{\max} i = \frac{ET}{4}$$

Where E=50, T=10us;

To select $\Delta_{\max} i$, the criteria was that is the 5% of I_{max}

$$\Delta_{\max} i = 5\% \text{ of } I_{max}.\ I_{max} = \frac{\sqrt{2}P_{max}}{V_{rms}} = 2{,}35A$$

$$L = \frac{50V * 10 * 10^{-6}s}{4 * 0.05 * 2.35A}$$

$$L = 1.06mH$$

The nearest commercial value of this inductor is $L_o = 1.14mH$

4.4 Design of the inputs filters of high and low H bridge converters.

In order to design the input filters it is necessary to simulate the inverter with a resistive load at maximum power in open loop and measure the inputs currents as it is shown Figure 4-7 where $L_{o1}=L_{o2}=0{,}5L$

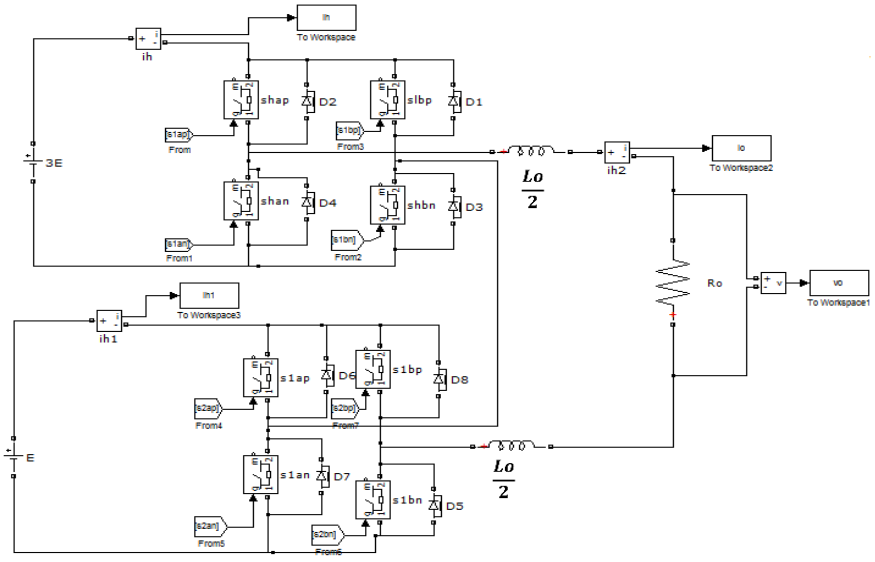

Figure 4-7 inverter in open loop off grid without input filter

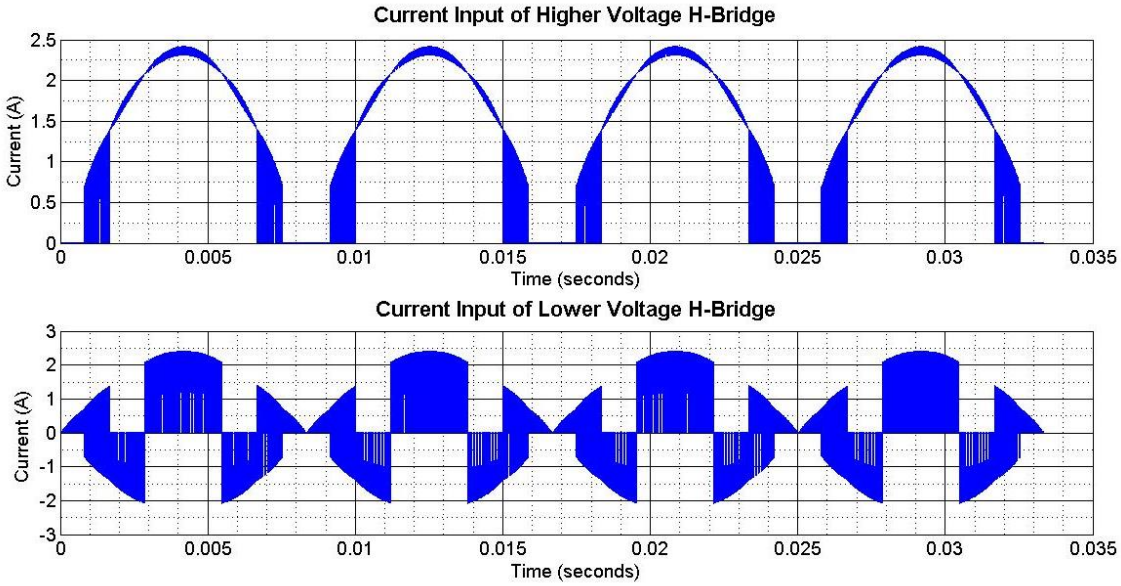

Figure 4-8 wave form of the input currents without input filter

Figure 4-8 shows the wave form of the input currents of the inverter in off grid with RC load without input filters.

Now it is necessary to know the harmonics components of each current. Frequency analyses of the input currents of the inverter without input filters are showed in Figure 4-9

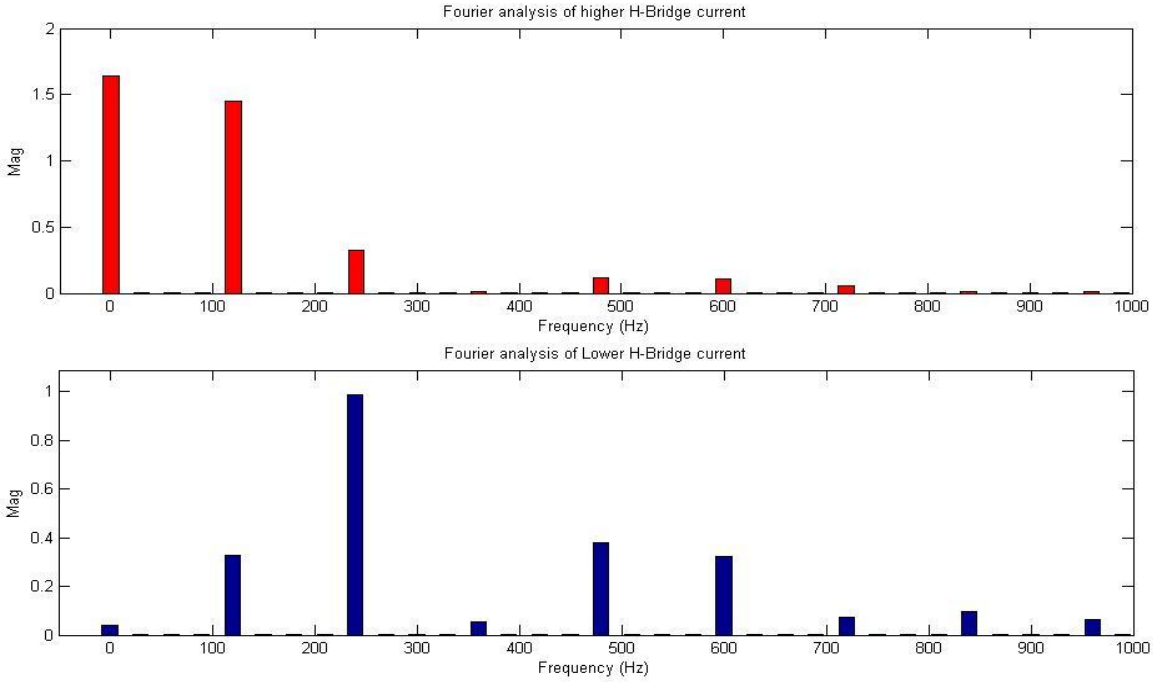

Figure 4-9 Frequency analysis

In the higher H-bridge the most harmonic component is at 120Hz I(120Hz)=1,5A and I(0Hz)=1,6A

The electric diagram of the circuit at 120Hz and 240Hz is described in **Figure 4-10**

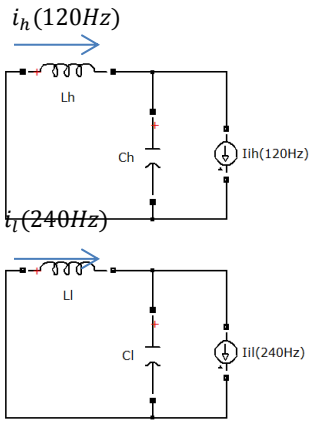

Figure 4-10 Circuits Higher HB at 120Hz and lower HB at 240Hz

Where L_h is the inductor of the input filter for the higher H-Bridge, C_h the capacitor of the input filter for the higher H-Bridge, L_l is the inductor of the input filter for the lower H-Bridge, C_l the capacitor of the input filter for the lower H-Bridge, $i_h(f)$ the harmonic component at f Hz of the input current of the Higher H-Bridge, $i_{ih}(f)$ the harmonic component at f Hz of the output current of the Higher H-Bridge, $i_l(f)$ the harmonic component at f Hz of the input current of the Lower H-Bridge, $i_{il}(f)$ the harmonic component at f Hz of the output current of the Lower H-Bridge.

If the maximum supply current at 120Hz in Higher H-Bridge is defined at 7% of the DC current

$$i_h(120Hz)L_h\omega j = \left(i_{ih}(120Hz) - i_h(120Hz)\right)\left(-\frac{j}{\omega C_h}\right)$$

$$i_h(120Hz) = \frac{i_{ih}(120Hz)}{\omega^2 L_h C_h + 1}$$

$$L_h C_h = \frac{1}{\omega^2}\left(\frac{i_{ih}(120Hz)}{i_h(120Hz)} - 1\right)$$

$$L_h C_h = 2.022 * 10^{-5}$$

$$\boldsymbol{L_h = 4.4mH; C_h = 4.7mF}$$

The series resistance R_{L_h} of the L_h is 0,2Ω.

To design the input lower H-Bridge filter due to the input current is almost 0, it is necessary a source able to receive current instantly , and the filter is a low pass filter of 2nd order with fc < 10% of the most significant harmonic. In order to ensure that the filter removes the component of 120Hz, fc is defined at 16Hz.

$$\sqrt{L_l C_l} = \frac{1}{2\pi f_c}$$

$$L_l C_l = 98.9 * 10^{-6}$$

$$\boldsymbol{L_l = 10mH; C_l 10mF}$$

The series resistance R_{L_l} of the L_l is 3,4Ω.

4.5 Simulation of the system in open loop with a RC load.

In this chapter the system will simulate with an RC load instead of the grid, this chapter is necessary to compare the simulation in open loop and the implementation.

Figure 4-12 describes the system to simulate, with and $R_o = 72\ \Omega$ to obtain the maximum power, and a $C_o = 2{,}2\mu F$, to obtain an output filter with a cut off frequency much bigger than ten times of power grid frequency (60Hz), and much smaller than 0,1 times of the switching frequency (100kHz). The system is simulated with losses in the inductors and switching devices.

In Figure 4-11 Vo(t) , Io(t) shows the output voltage V_o and output current I_o

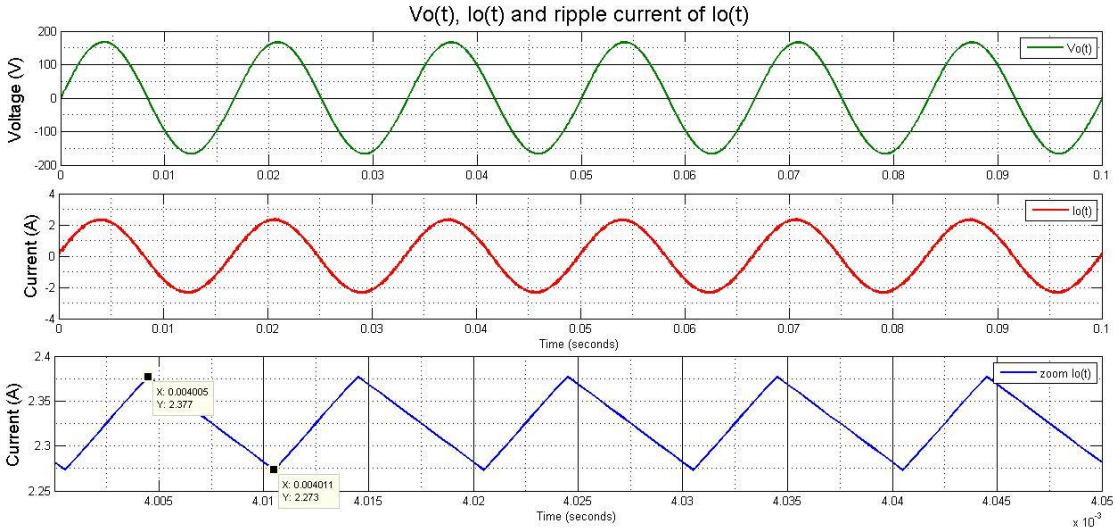

Figure 4-11 Vo(t) , Io(t)

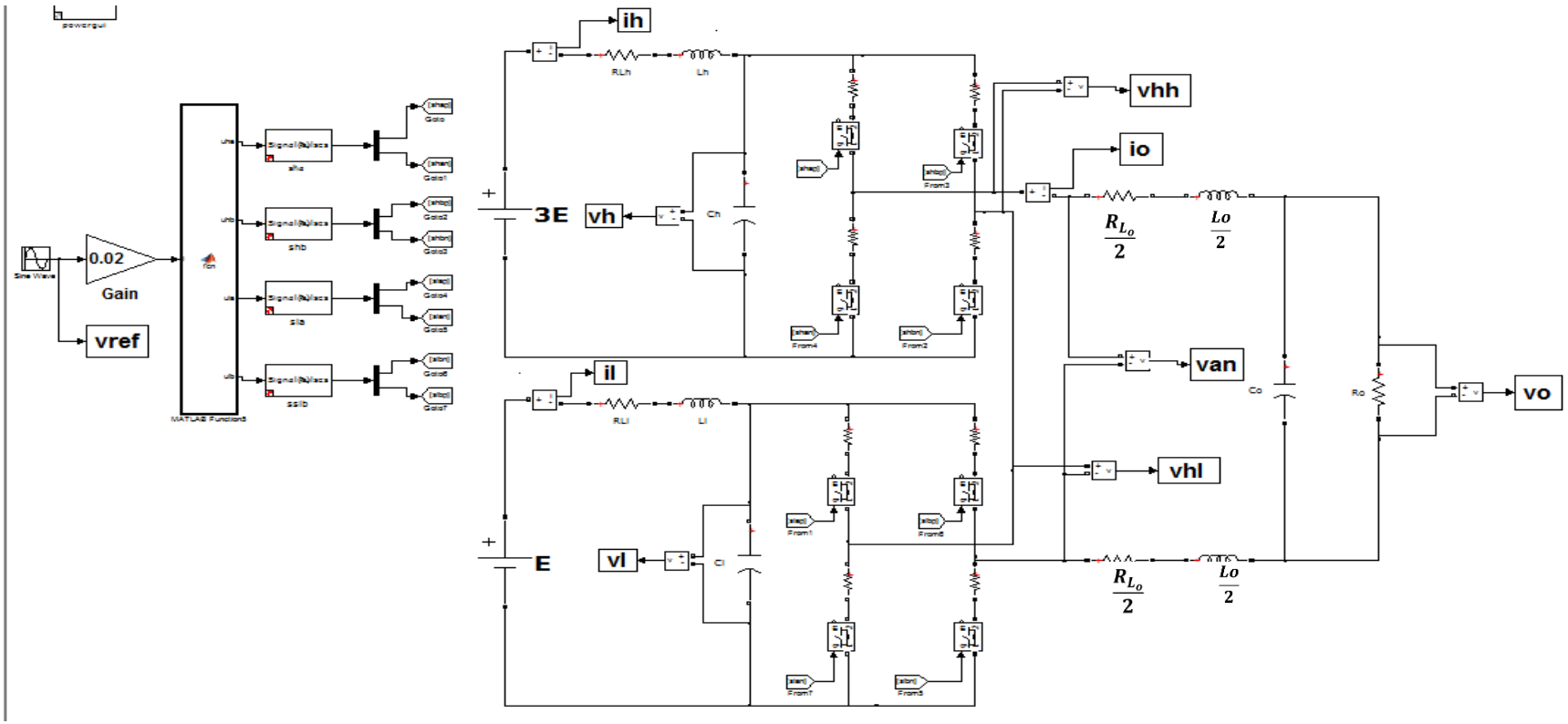

Figure 4-12 inverter wit RC load in open loop

Notice that the ripple current in **Figure 4-11** is very small. This satisfies the allowed ripple current in the output, and notice that the output voltage v_o do not have ripple.

Figure 4-13 *$V_{hh}(t)$, $V_{hl}(t)$, $V_{an}(t)$* shows the voltage on each H-bridge and the output of the total H-Bridges. Notice that the levels are clearly defined.

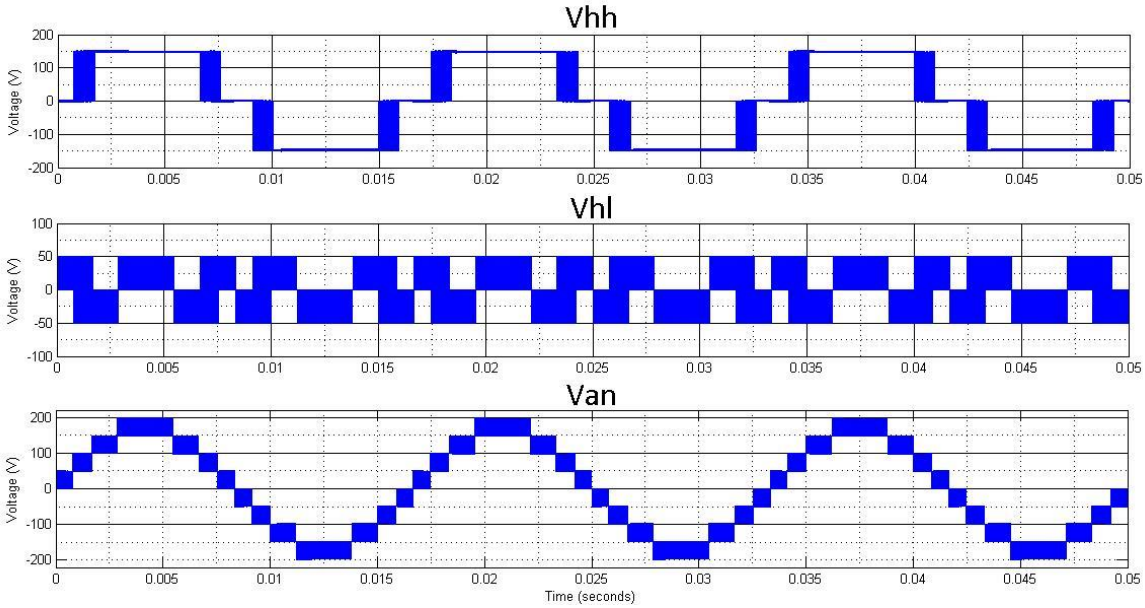

Figure 4-13 *$V_{hh}(t)$, $V_{hl}(t)$, $V_{an}(t)$*

Figure 4-14 shows the voltage input on each H-Bridge, a small voltage ripple is generated due to the input filters that the controller has to compensate

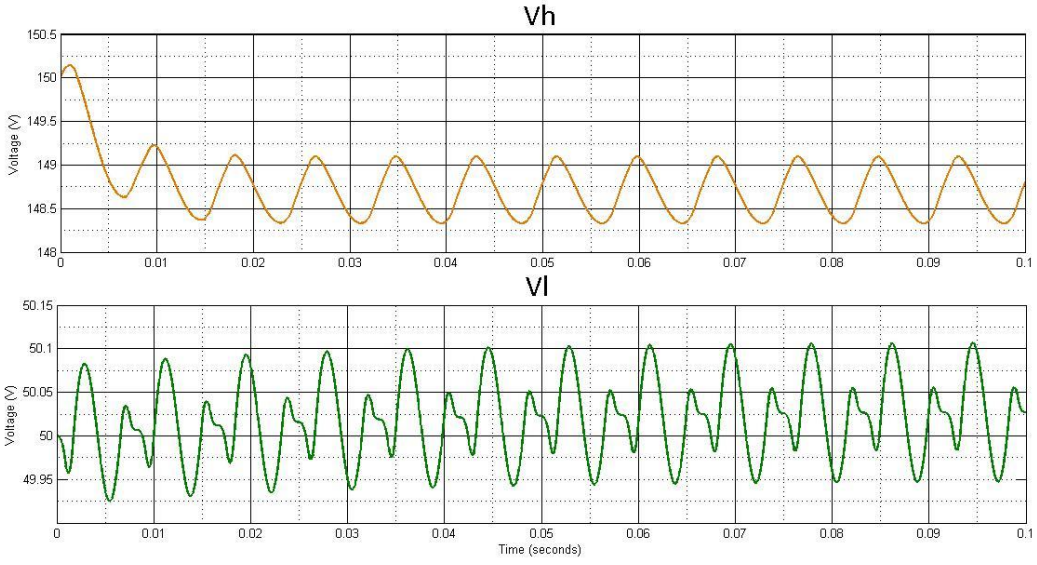

Figure 4-14Vh(t), Vl(t)

4.6 Model of the inverter with input filters

In this chapter the inverter will be modeled in state variables

Suppose S_x a vector defined in R^2 where $S_x = (S_h , S_l)$ where $S_h = S_{ha} - S_{hb}$, and $S_l = S_{la} - S_{lb}$.

The Table 4.1 math description of inverter with input filter shows the math description of all the possible values of S_x

$S_x = (S_h, S_l)$	Model
$(\mathbf{1}, \mathbf{1})$	$\begin{bmatrix} 3E = L_h \frac{di_h}{dt} + R_{L_h} i_h + v_h \\ i_h = C_h \frac{dv_h}{dt} + i_o \\ E = L_l \frac{di_l}{dt} + R_{L_l} i_l + v_l \\ i_l = C_l \frac{dv_l}{dt} + i_o \\ v_h + v_l = L_o \frac{di_o}{dt} + (R_{Lo} + 2R_{dsh} + 2R_{dsl}) i_o + v_{ac} \end{bmatrix}$
$(\mathbf{1}, \mathbf{0})$	$\begin{bmatrix} 3E = L_h \frac{di_h}{dt} + R_{L_h} i_h + v_h \\ i_h = C_h \frac{dv_h}{dt} + i_o \\ E = L_l \frac{di_l}{dt} + R_{L_l} i_l + v_l \\ i_l = C_l \frac{dv_l}{dt} \\ v_h = L_o \frac{di_o}{dt} + (R_{Lo} + 2R_{dsh} + 2R_{dsl}) i_o + v_{ac} \end{bmatrix}$
$(\mathbf{1}, -\mathbf{1})$	$\begin{bmatrix} 3E = L_h \frac{di_h}{dt} + R_{L_h} i_h + v_h \\ i_h = C_h \frac{dv_h}{dt} + i_o \\ E = L_l \frac{di_l}{dt} + R_{L_l} i_l + v_l \\ i_l = C_l \frac{dv_l}{dt} - i_o \\ v_h - v_l = L_o \frac{di_o}{dt} + (R_{Lo} + 2R_{dsh} + 2R_{dsl}) i_o + v_{ac} \end{bmatrix}$
$(\mathbf{0}, \mathbf{1})$	$\begin{bmatrix} 3E = L_h \frac{di_h}{dt} + R_{L_h} i_h + v_h \\ i_h = C_h \frac{dv_h}{dt} \\ E = L_l \frac{di_l}{dt} + R_{L_l} i_l + v_l \\ i_l = C_l \frac{dv_l}{dt} + i_o \\ v_l = L_o \frac{di_o}{dt} + (R_{Lo} + 2R_{dsh} + 2R_{dsl}) i_o + v_{ac} \end{bmatrix}$

$(\mathbf{0},\mathbf{0})$	$\begin{bmatrix} 3E = L_h\frac{di_h}{dt} + R_{L_h}i_h + v_h \\ i_h = C_h\frac{dv_h}{dt} \\ E = L_l\frac{di_l}{dt} + R_{L_l}i_l + v_l \\ i_l = C_l\frac{dv_l}{dt} \\ 0 = L_o\frac{di_o}{dt} + (R_{Lo} + 2R_{dsh} + 2R_{dsl})i_o + v_{ac} \end{bmatrix}$
$(\mathbf{0},-\mathbf{1})$	$\begin{bmatrix} 3E = L_h\frac{di_h}{dt} + R_{L_h}i_h + v_h \\ i_h = C_h\frac{dv_h}{dt} \\ E = L_l\frac{di_l}{dt} + R_{L_l}i_l + v_l \\ i_l = C_l\frac{dv_l}{dt} - i_o \\ -v_l = L_o\frac{di_o}{dt} + (R_{Lo} + 2R_{dsh} + 2R_{dsl})i_o + v_{ac} \end{bmatrix}$
$(-\mathbf{1},\mathbf{1})$	$\begin{bmatrix} 3E = L_h\frac{di_h}{dt} + R_{L_h}i_h + v_h \\ i_h = C_h\frac{dv_h}{dt} - i_o \\ E = L_l\frac{di_l}{dt} + R_{L_l}i_l + v_l \\ i_l = C_l\frac{dv_l}{dt} + i_o \\ -v_h + v_l = L_o\frac{di_o}{dt} + (R_{Lo} + 2R_{dsh} + 2R_{dsl})i_o + v_{ac} \end{bmatrix}$
$(-\mathbf{1},\mathbf{0})$	$\begin{bmatrix} 3E = L_h\frac{di_h}{dt} + R_{L_h}i_h + v_h \\ i_h = C_h\frac{dv_h}{dt} - i_o \\ E = L_l\frac{di_l}{dt} + R_{L_l}i_l + v_l \\ i_l = C_l\frac{dv_l}{dt} \\ -v_h = L_o\frac{di_o}{dt} + (R_{Lo} + 2R_{dsh} + 2R_{dsl})i_o + v_{ac} \end{bmatrix}$
$(-\mathbf{1},-\mathbf{1})$	$\begin{bmatrix} 3E = L_h\frac{di_h}{dt} + R_{L_h}i_h + v_h \\ i_h = C_h\frac{dv_h}{dt} - i_o \\ E = L_l\frac{di_l}{dt} + R_{L_l}i_l + v_l \\ i_l = C_l\frac{dv_l}{dt} - i_o \\ -v_h - v_l = L_o\frac{di_o}{dt} + (R_{Lo} + 2R_{dsh} + 2R_{dsl})i_o + v_{ac} \end{bmatrix}$

Table 4.1 math description of inverter with input filter

Accordingly the model can be written as

$$\begin{bmatrix} \dot{i}_h \\ \dot{v}_h \\ \dot{i}_l \\ \dot{v}_l \\ \dot{i}_o \end{bmatrix} = \begin{bmatrix} -\frac{R_{L_h}}{L_h} & -\frac{1}{L_h} & 0 & 0 & 0 \\ \frac{1}{C_h} & 0 & 0 & 0 & 0 \\ 0 & 0 & -\frac{R_{L_l}}{L_l} & 0 & 0 \\ 0 & 0 & \frac{1}{C_l} & 0 & 0 \\ 0 & 0 & 0 & 0 & -\frac{Rx}{L_o} \end{bmatrix} \begin{bmatrix} i_h \\ v_h \\ i_l \\ v_l \\ i_o \end{bmatrix} + \begin{bmatrix} 0 & 0 \\ -\frac{i_o}{C_h} & 0 \\ 0 & 0 \\ 0 & -\frac{i_o}{C_l} \\ \frac{v_h}{2L_o} & \frac{v_l}{2L_o} \end{bmatrix} \begin{bmatrix} S_h \\ S_l \end{bmatrix} + \begin{bmatrix} \frac{3E}{L_h} \\ 0 \\ \frac{E}{L_l} \\ 0 \\ -\frac{v_{ac}}{2L_o} \end{bmatrix} \quad \text{Eq. 4-5}$$

Where $R_x = R_{Lo} + 2R_{dsh} + 2R_{dsl}$

The average model is:

$$\begin{bmatrix} \dot{i}_h \\ \dot{v}_h \\ \dot{i}_l \\ \dot{v}_l \\ \dot{i}_o \end{bmatrix} = \begin{bmatrix} -\frac{R_{L_h}}{L_h} & -\frac{1}{L_h} & 0 & 0 & 0 \\ \frac{1}{C_h} & 0 & 0 & 0 & 0 \\ 0 & 0 & -\frac{R_{L_l}}{L_l} & 0 & 0 \\ 0 & 0 & \frac{1}{C_l} & 0 & 0 \\ 0 & 0 & 0 & 0 & -\frac{Rx}{L_o} \end{bmatrix} \begin{bmatrix} i_h \\ v_h \\ i_l \\ v_l \\ i_o \end{bmatrix} + \begin{bmatrix} 0 & 0 \\ -\frac{i_o}{C_h} & 0 \\ 0 & 0 \\ 0 & -\frac{i_o}{C_l} \\ \frac{v_h}{2L_o} & \frac{v_l}{2L_o} \end{bmatrix} \begin{bmatrix} u_h \\ u_l \end{bmatrix} + \begin{bmatrix} \frac{3E}{L_h} \\ 0 \\ \frac{E}{L_l} \\ 0 \\ -\frac{v_{ac}}{2L_o} \end{bmatrix} \quad \text{Eq. 4-6}$$

According to Eq. 4-6 the inverter can be modeled as the circuit shown in Figure 4-15

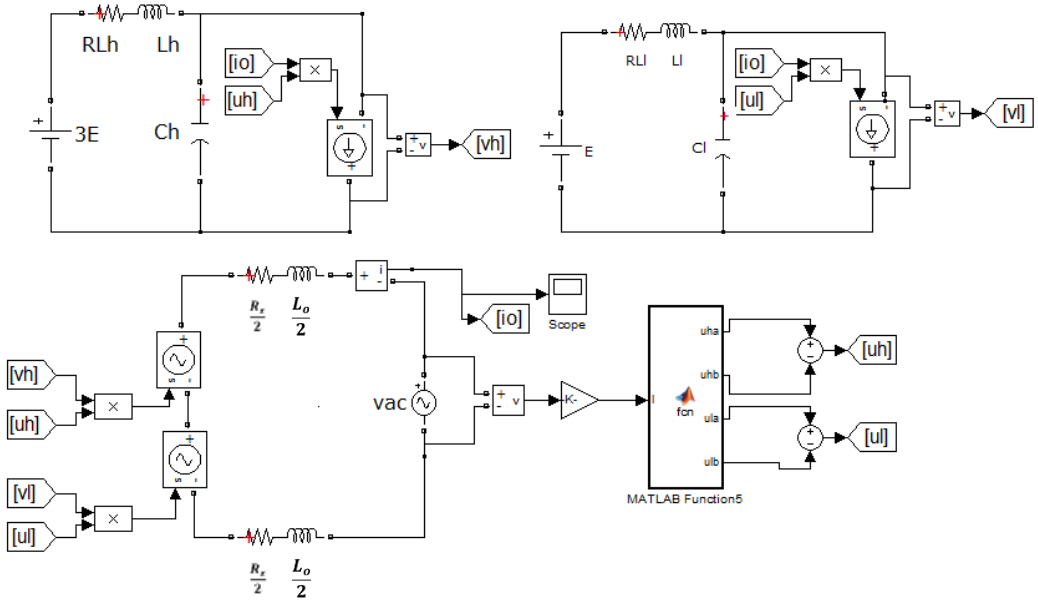

Figure 4-15 average model

Figure 4-16 average model vs switching model shows the switching model and the average model with an input u=1,014v_{ac} and can be inferred that the average model proposed is a very good model of THMI.

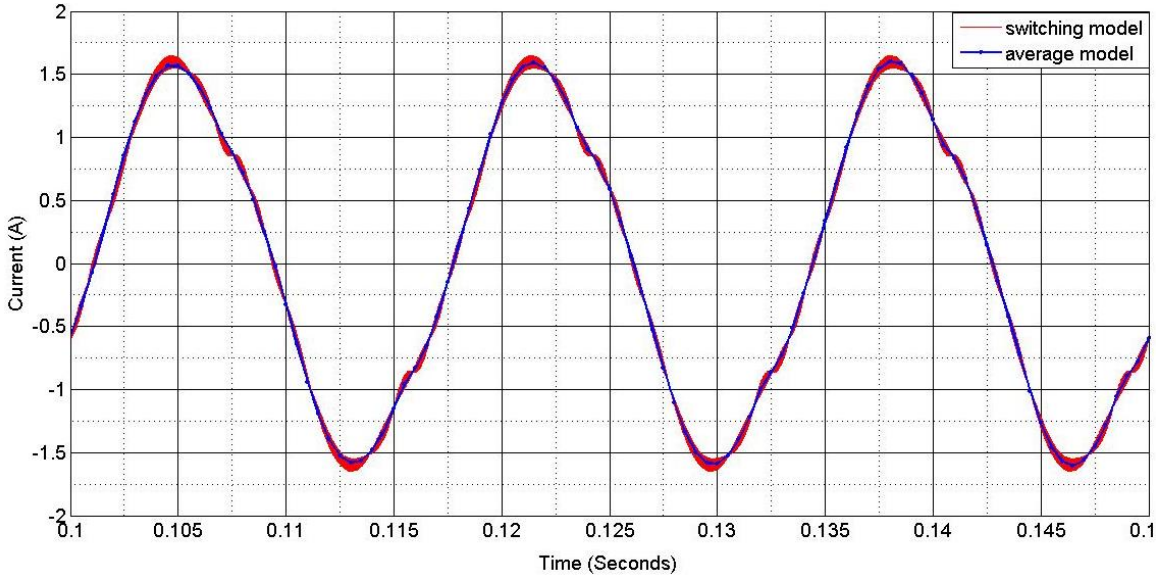

Figure 4-16 average model vs switching model

$$e_{rms} = 24{,}62\ x10^{-3}\ A$$

e_{rms} is the RMS error between the output current of the switching circuit with input filters and the output current of the average model with inputs filters during a period of 16,66ms.

Consider that the RMS error is much lower than the amplitude of the currents; the model can be accepted as a very good model.

4.7 Model of the inverter without input filters

For complexity reasons is better to take the average model of the inverter without inputs filter instead of linearizing the average model.

The model equation is showed in

$$I_o(s) = \left((3U_h(s) + U_l(s)) - \frac{V_{ac}(s)}{E}\right)\frac{E}{L_o s + R_x} \qquad \text{Eq. 4-7}$$

If $U(s) = 3U_h(s) + U_l(s)$

$$I_o(s) = \left(U(s) - \frac{V_{ac}(s)}{E}\right)\frac{E}{L_o s + R_x}$$

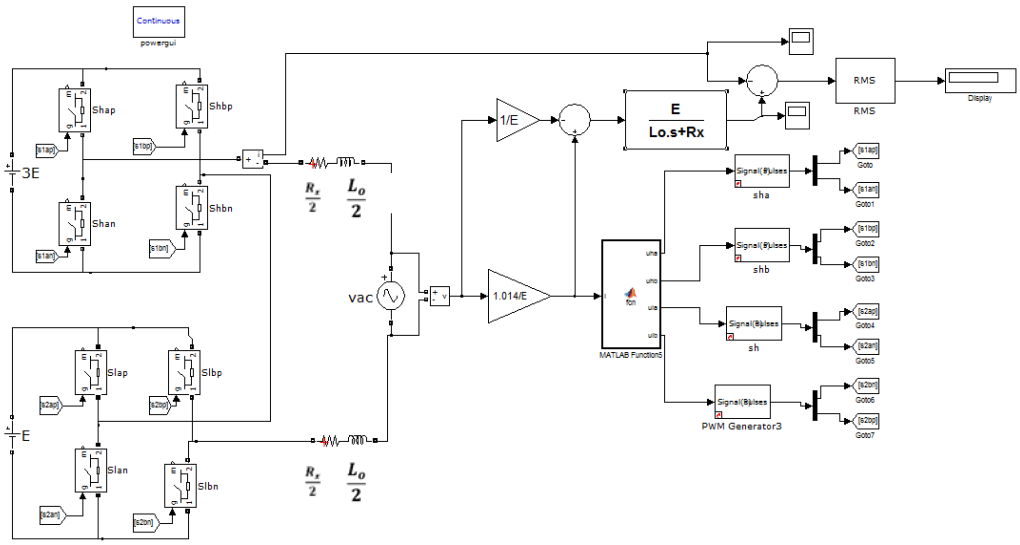

Figure 4-17 block diagram of average model and switching model without inputs filters

Figure 4-17 block diagram of average model and switching model without inputs filtersshows the model and the switching circuit

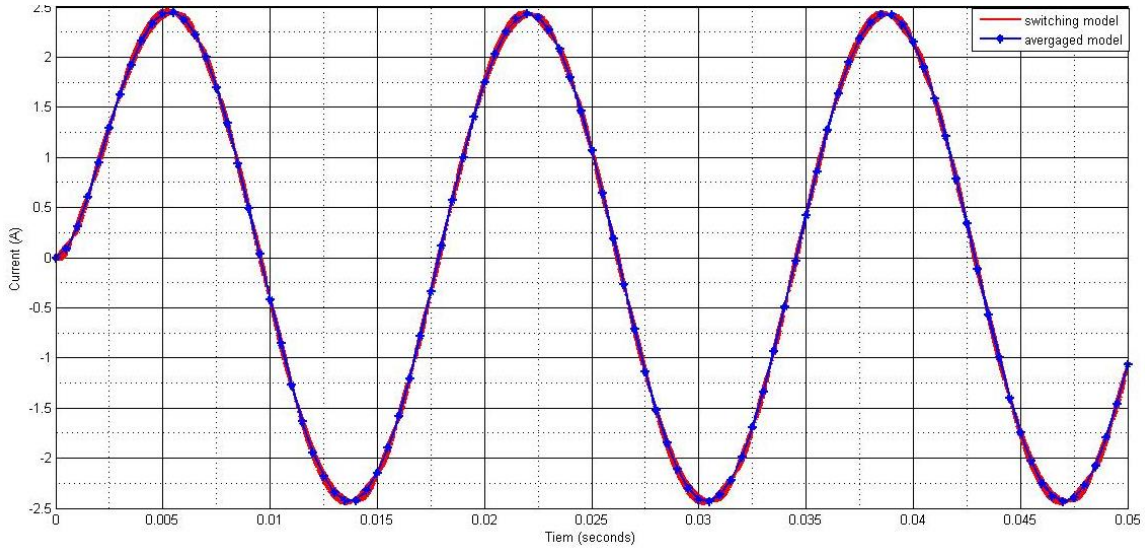

Figure 4-18 Average model Vs switching model without inputs filter

Figure 4-18 Average model Vs switching model without inputs filter shows the wave form of the average model and the switching circuit

$$e_{rms} = 24{,}15\ x10^{-3}\ A$$

e_{rms} is the RMS error between the output current of the switching circuit without input filters and the output current of the average model without inputs filters during a period of 16,66ms.

Consider that the RMS error is much lower than the amplitude of the currents, the model can be accepted as a very good model.

4.8 Design and simulation of the linear controller

The average model with input filters can be modeled as the invert without input filter plus an uncertainty voltage ΔV,

According the last state equation is described as:

$$L_o \frac{di_o}{dt} = v_h(t)u_h(t) + v_l(t)u_l(t) - R_x i_o(t) - v_{ac}(t)$$
$$v_h(t) = 3E + \Delta v_h(t);\ \ v_l(t) = E + \Delta v_l(t);$$

$$L_o \frac{di_o}{dt} = E\big(3u_h(t) + u_l(t)\big) - R_x i_o(t) - v_{ac}(t) + \big(\Delta v_h(t)u_h(t) + \Delta v_l(t)u_l(t)\big)$$
$$\Delta v(t) = \Delta v_h(t)u_h(t) + \Delta v_l(t)u_l(t); u(t) = 3u_h(t) + u_l(t)$$

$$\boldsymbol{L_o \frac{di_o}{dt} = Eu(t) - R_x i_o(t) - v_{ac}(t) + \Delta v(t)} \qquad \text{Eq. 4-8}$$

$$\boldsymbol{I_o(s) = \left(U(s) - \frac{V_{ac}(s)}{E}\right)\left(\frac{E}{L_o s + R_x}\right) + \frac{\Delta V(s)}{L_o s + R_x}} \qquad \text{Eq. 4-9}$$

A Proportional controller never reaches a steady-state error of 0. Integral controller could not adjust *zita* without altering the natural frequency of the feedback system. A controller with a derivative action amplifies the noise measurement of the sensor resulting in an unstable loop.

For this reason a Proportional-Integral (PI) controller would be the only viable option for linear control.

Due that the 11-th harmonic is the last significant harmonic of the grid voltage, the linear controller will be defined in *SISOTOOL* with the criteria that the fc will be equal at on decade after the 11-th Harmonics.

$$G_c(s) = 0.9 + \frac{450}{s}$$

$G_c(s)$ is the controller selected that satisfies the criteria.

To implement the PI controller in Digital signals processor (DSP), is necessary to convert into a Z transfer function.

To convert into a Z transfer function is necessary to define a sampling frequency of all the variables (v_o, i_o, v_i). This sampling frequency must be equal or a sub-multiple to the switching frequency. If the sampling frequency is the same of the switching frequency (100kHz), the

processing time is not enough, because the complexity of the process to conversion of *u(t)* to the duty cycle of each MOSFET , for this reason the sample time, Ts, of all the variables is 20µs.

With the sample time, Ts, defined the Z transform of the linear controller is:

$$G_{cd}(z) = 0.9\frac{(1-0.99z^{-1})}{1-z^{-1}}$$

In order to generate the reference current, i_{ref} it is assumed that the signal $v_{ac}(t)$ *equals* $v_{ac}(nT+t)$, where T is the period of the voltage waveform, and *n is a positive integer*. Due to the sample time is 20 µs, the last period of the voltage signals is saved in an array with a size of 84 samples, that is uploading constantly. Then the array is scaled and the index of the current position on the array is slid according to the desired phase displacement.

If the phase displacement is too much, the power supplies of the inverter could have negative instant current and the power supplies used in this project do not allow that. For this reason the maximum power factor is 0.7, and obtains a maximum and minimum phase displacement of ±45˚.

Figure 4-19 linear controller block diagram shows the block diagram of the average model of the inverter controlled by the linear controller.

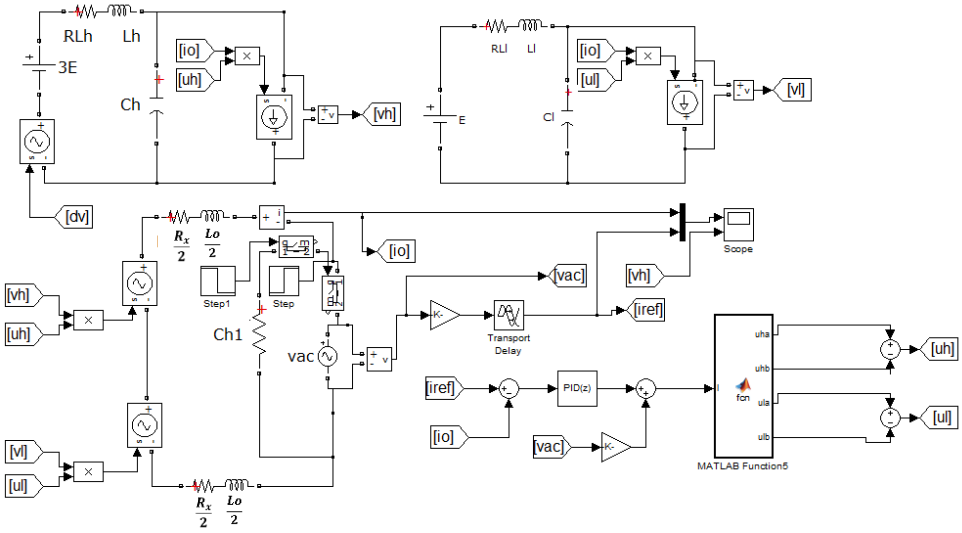

Figure 4-19 linear controller block diagram

Figure 4-20 shows the waveform of the linear controller changing phase and magnitude of the reference current.

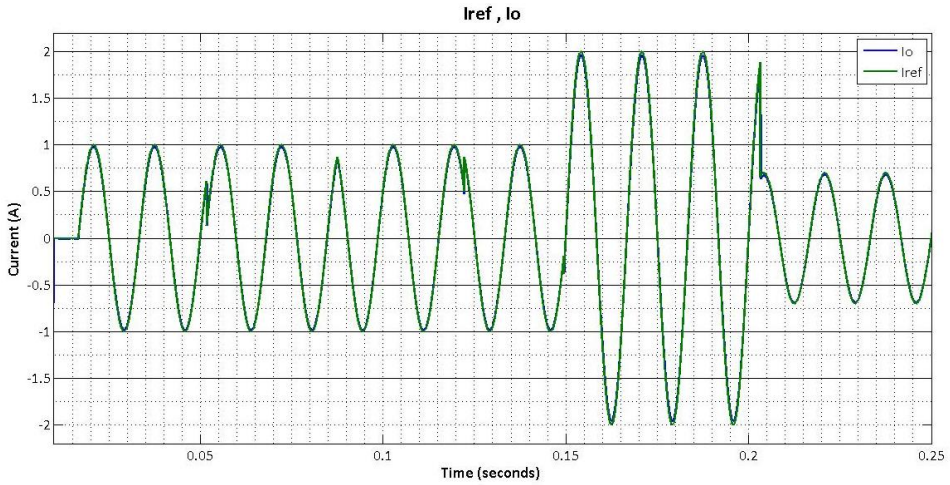

Figure 4-20 Changes on phase and magnitude of Iref with linear controller

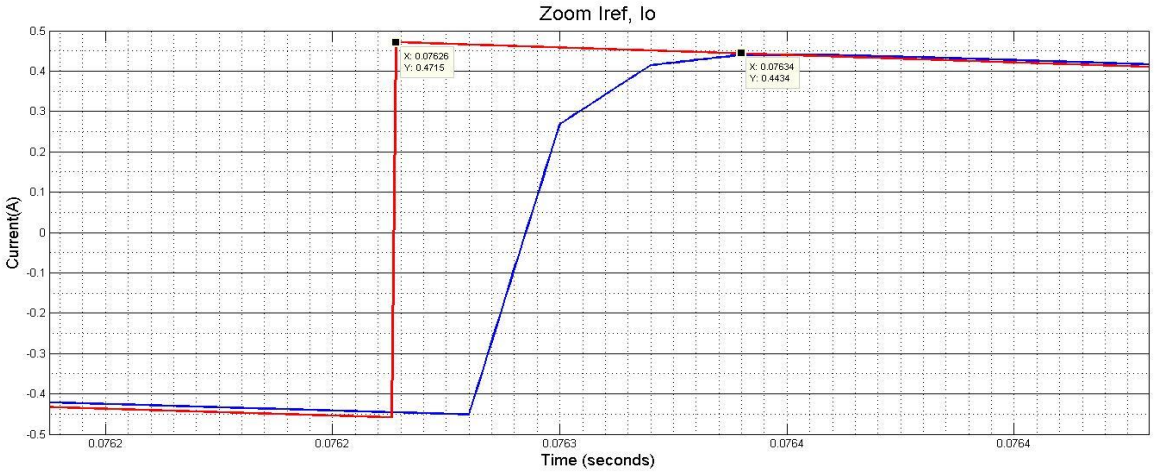

Figure 4-21 zoom of Iref, Io

Figure 4-21 shows a zoom of I_{ref} and I_o and the transient response time is 80 µs

Figure 4-22 shows the waveform with the linear controller with a disturbance in the power supply of the higher H-bridge. Notice that if the voltage disturbance increases, I_o do not reach I_{ref}

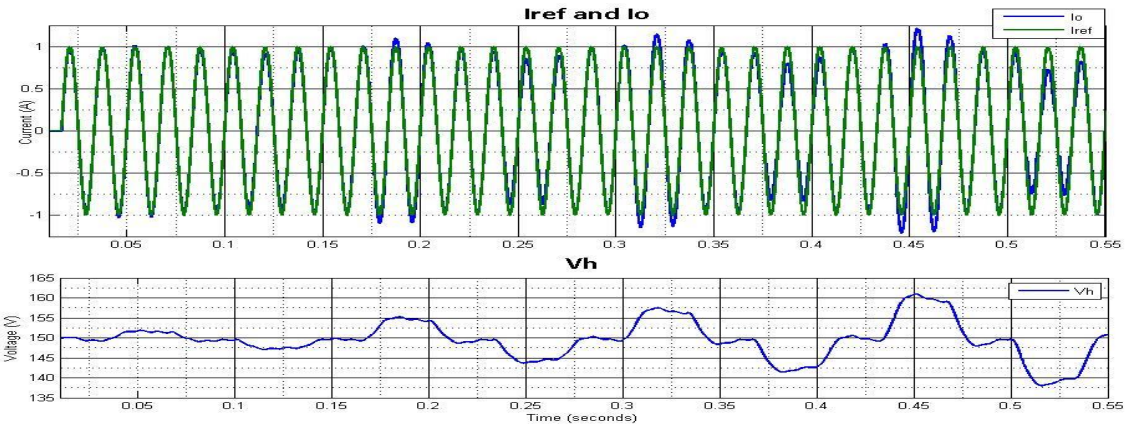

Figure 4-22 Disturbance in Vh with linear controller

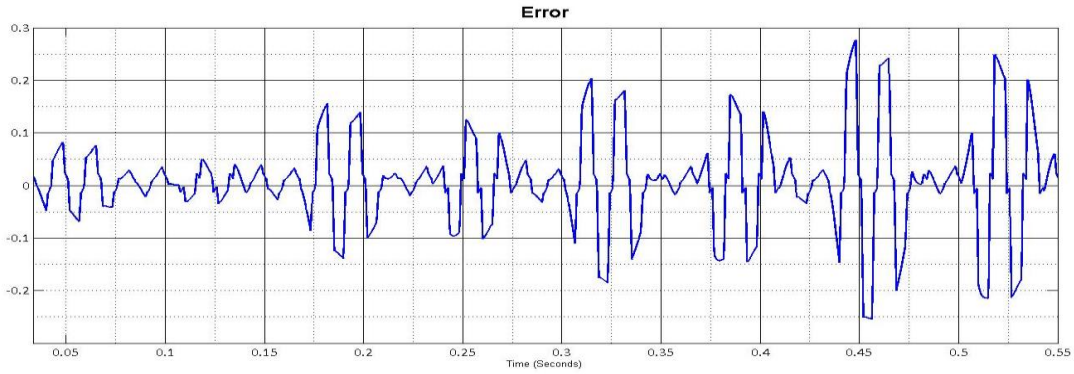

Figure 4-23 Error in linear controller

Figure 4-23 shows the waveform of the error. Notice that the maximum error is 0,27 A.

The $e_{rms} = 99{,}8x10^{-3}\ A$

The Total Harmonic Distortion (THD) of i_o without disturbance at nominal current (1,66Arms) on phase in linear control is 2.38%.

4.9 Design and simulation of the nonlinear controller

The nonlinear controller is designed with Sliding Mode Control using an integral surface

Accordingly:

$$e(t) = i_o(t) - i_{ref}(t)$$

Suppose a sliding surface S_1 as:

$$S_1(e) = e(t) + e_0 + \alpha \int_0^t e(\tau)d\tau \qquad \text{Eq. 4-10}$$

$$where\ e_0 = e(0)$$

Suppose a Lyapunov function of S_1 as:

$$V(S_1) = \frac{1}{2}S_1^2$$

The Derivative of the V(s) is:

$$\dot{V}(S_1) = S_1\dot{S_1}$$

$$\dot{V}(S_1) = S_1(\dot{e}(t) + \alpha e(t) - \alpha e_0) \quad \text{Eq. 4-11}$$

$$\dot{e}(t) = \dot{\iota_o}(t) - \dot{\iota_{ref}}(t)$$

According to **Eq. 4-8 :**

$$\dot{e}(t) = \frac{\boldsymbol{E}}{\boldsymbol{L_o}}\boldsymbol{u(t)} - \frac{\boldsymbol{R_x}}{\boldsymbol{L_o}}\boldsymbol{i_o(t)} - \frac{\boldsymbol{1}}{\boldsymbol{L_o}}\boldsymbol{v_{ac}(t)} + \frac{\boldsymbol{1}}{\boldsymbol{L_o}}\Delta\boldsymbol{v(t)} - \dot{\iota_{ref}}(t) \quad \text{Eq. 4-12}$$

If **Eq. 4-12** is used in **Eq. 4-11**

$$\dot{V}(S_1) = S_1\left(\frac{E}{L_o}u(t) - \frac{R_x}{L_o}i_o(t) - \frac{1}{L_o}v_{ac}(t) + \frac{1}{L_o}\Delta v(t) - \dot{\iota_{ref}}(t) + \alpha e(t) - \alpha e_0\right) < 0$$

$$\dot{V}(S_1) = \frac{S_1}{L_o}\left(Eu(t) - R_x i_o(t) - v_{ac}(t) + \Delta v(t) - 2L_o\dot{\iota_{ref}}(t) + 2L_o\alpha e(t) - L_o\alpha e_0\right) < 0 \quad \text{Eq. 4-13}$$

$u(t)$ is defined as the sum of 2 different signals:

$$u(t) = u_1(t) + u_2(t)$$

$u_1(t)$ nullifies all the terms except the uncertainly variations.

$$u_1(t) = \frac{1}{E}(R_x i_o(t) + v_{ac}(t) + L_o i_{ref}(t) - L_o\alpha e(t) + L_o\alpha e_0$$

Replacing $u_1(t)$ in **Eq. 4-13**

$$\dot{V}(S_1) = S_1\left(Eu_2(t) + \Delta v(t)\right) < 0$$

$u_2(t)$ try to stabilize the system for uncertainly variations or disturbance and it is defined as:

$$u_2(t) = -\frac{\gamma}{E}S_1 \quad \text{Eq. 4-14}$$

Replacing **Eq. 4-14** in **Eq. 4-13**:

$$\dot{V}(S_1) = S_1\left(-\gamma S_1 + \Delta v(t)\right) < 0$$

$$\left(S_1 > 0 \ \wedge S_1 > \frac{\Delta v(t)}{\gamma}\right) \vee \left(S_1 < 0 \ \wedge S_1 < \frac{\Delta v(t)}{\gamma}\right) \qquad \text{Eq. 4-15}$$

Replacing **Eq. 4-10** in **Eq. 4-15**

$$\left(e(t) + e_0 + \alpha \int_0^t e(\tau)d\tau > 0 \ \wedge \ e(t) + e_0 + \alpha \int_0^t e(\tau)d\tau > \frac{\Delta v(t)}{\gamma}\right) \vee$$
$$\left(e(t) + e_0 + \alpha \int_0^t e(\tau)d\tau < 0 \ \wedge \ e(t) + e_0 + \alpha \int_0^t e(\tau)d\tau < \frac{\Delta v(t)}{\gamma}\right)$$

Solving the differential inequality:

$$\left(e(t) > -e_0 e^{-\alpha t} \wedge \ e(t) > \left(-e_0 + \frac{\Delta v(t)}{\gamma}\right)e^{-\alpha t}\right) \vee$$
$$\left(e(t) < -e_0 e^{-\alpha t} \wedge \ e(t) < \left(-e_0 + \frac{\Delta v(t)}{\gamma}\right)e^{-\alpha t}\right)$$

Figure 4-24 shows with blue color the region with unknown stability but this zone tend to 0.

S_1 will be stable in a Lyapunov sense while $\lim_{t\to\propto} \Delta v(t) \neq \propto$.

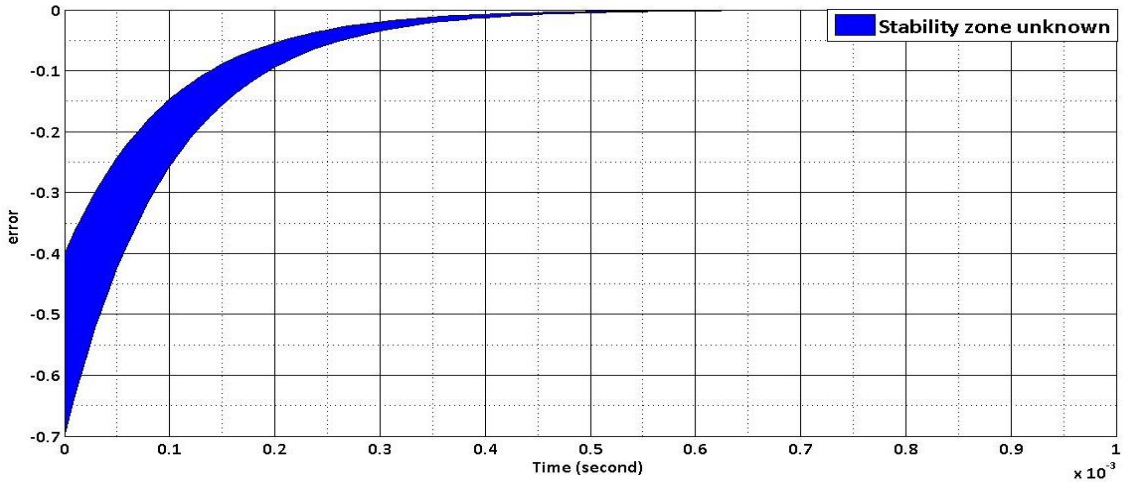

Figure 4-24

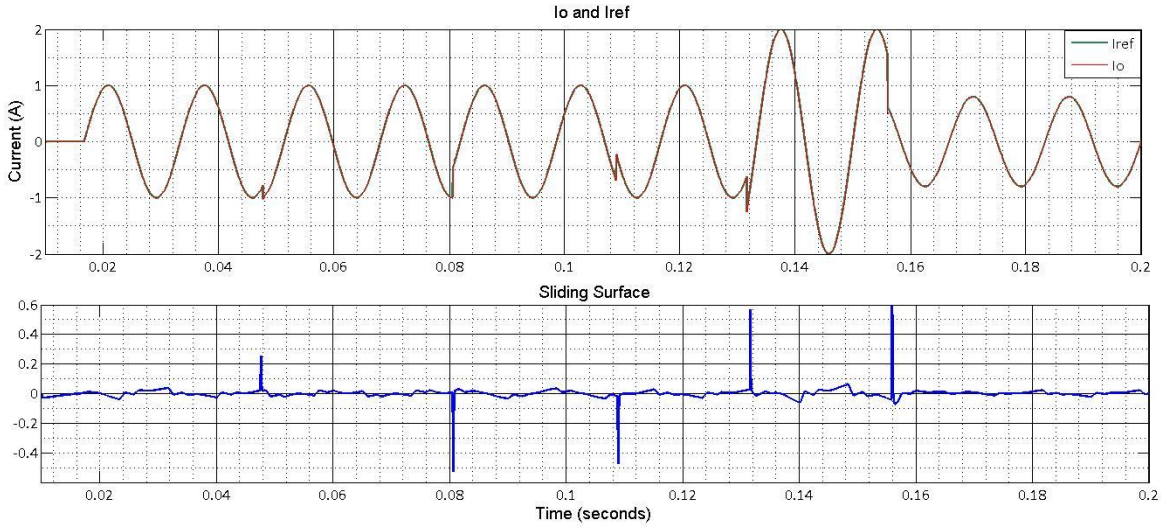

Figure 4-25 Changes on phase and magnitude of Iref with sliding mode controller

Figure 4-25 Changes on phase and magnitude of Iref with sliding mode controllershows I_o if the amplitude and the phase of I_{ref} is changed.

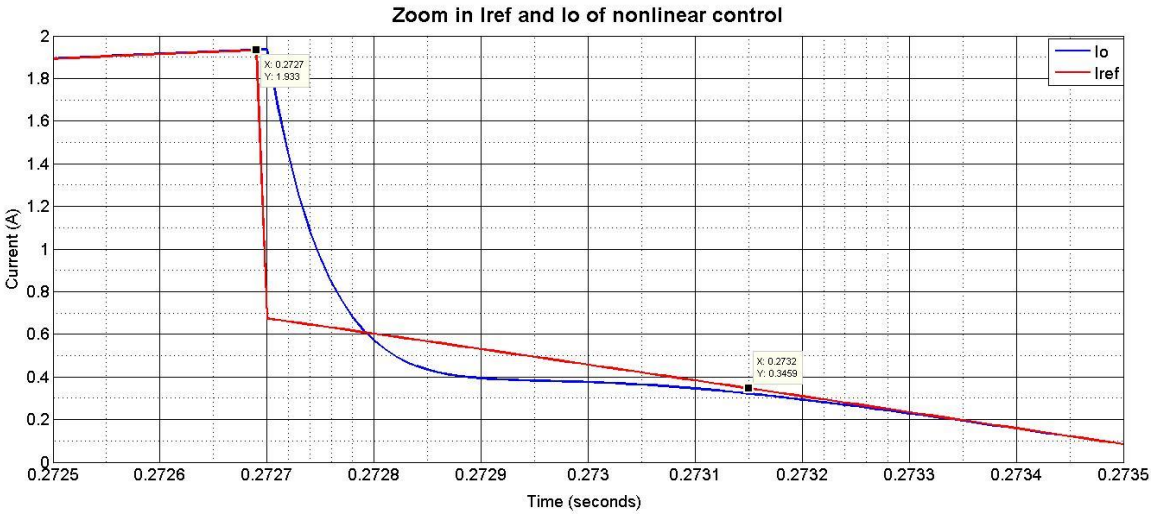

Figure 4-26 zoom in Io and Iref

Figure 4-26 shows a zoom of I_{ref} and I_o and the transient responses time is 450µs.

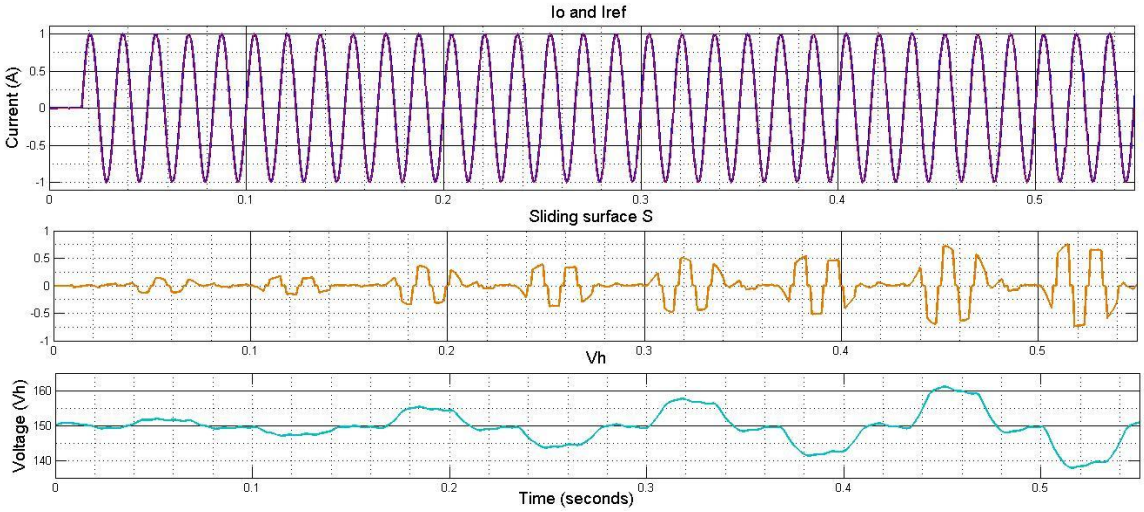

Figure 4-27 Disturbance in Vh with Sliding mode control

Figure 4-27 shows the waveform of the nonlinear controller with a disturbance in the power supply of the higher H-bridge. Notice that if the voltage disturbance increase, always I_o reach I_{ref}

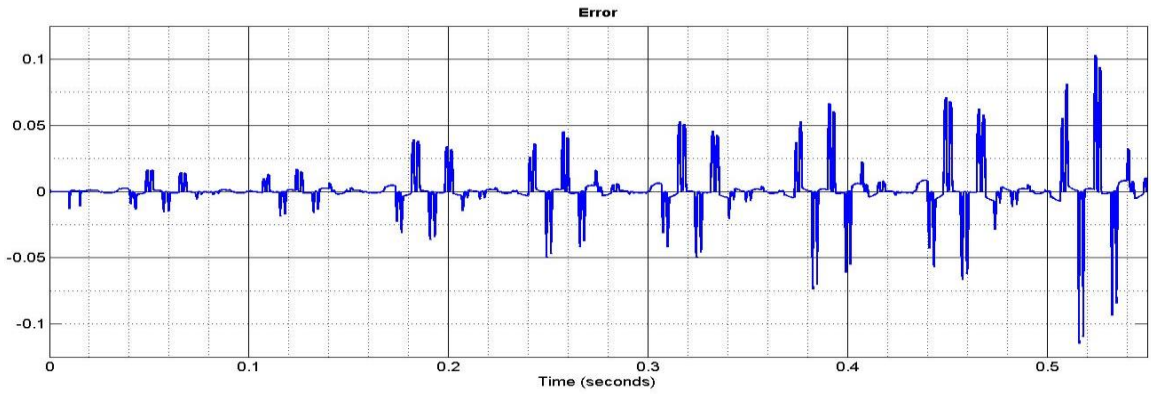

Figure 4-28 Error in nonlinear control

Figure 4-28 shows the waveform of the error with the disturbance in V_h, described in Figure 4-27. Notice that the maximum error is 0,1 A.

The $e_{rms} = 18x10^{-3}\ A$

The Total Harmonic Distortion (THD) of io without disturbance at nominal current (1.66 Arms) on phase in nonlinear control is 1.44%.

Controller	***Transient response time***	***Max error in disturbance (e_{max})***	e_{rms}	**THD**
PI controller	80µs	0,27	$99,8x10^{-3}$	2,38%
Sliding mode control	450 µs	0,1	$18x10^{-3}$	1,44%

Table 4.2 Comparative analysis of the controllers

In **Table 4.2** shows the main features of both controllers and indicate that both have good transient responses; although PI controller is faster, this is not very important because both controllers respond fast enough to control the inverter. The difference is in magnitude of the errors and THD. PI controller has a max error and e_{rms} much bigger than the Sliding mode control, and THD is bigger too. It can be inferred that the sliding mode control is better for the inverter,

5 Implementation:

This chapter shows the implementation process, elements and techniques of the inverter and both controllers.

To implement the hardware, 4 main circuits were designed: higher H-Bridge card, Lower H-Bridge card, Sensing card and output filter card. In Annex 1 shows the schematic of whole the inverter.

Figure 5-1 Hardware of the inverteris a photo of the hardware of the inverter.

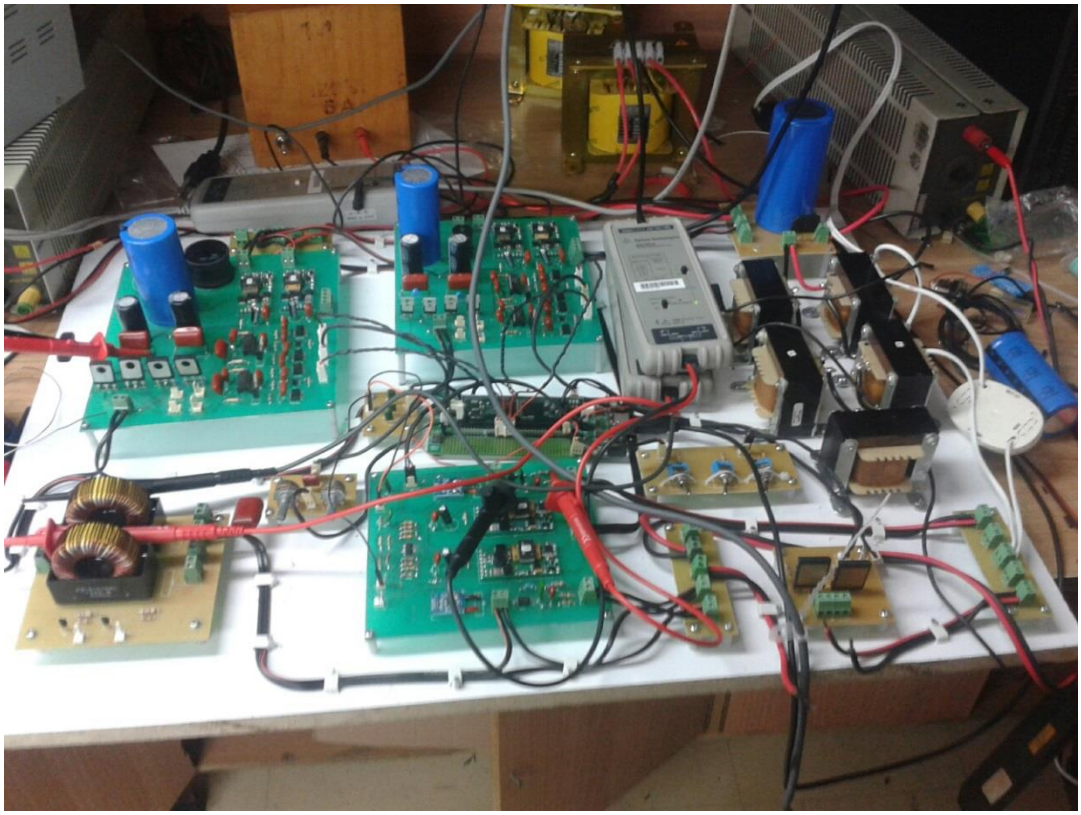

Figure 5-1 Hardware of the inverter

5.1 Inverters with RC load in open loop.

Figure 5-2 shows the output voltage of each H-Bridge (yellow HV and red LV) and the total output of the H-Bridges (blue) (VH_l, VH_h,V_{an}). Notice that due to the dead time many intervals of the waveform of V_{an} have a considerable overshoot, this occurs because in this interval one H-Bridge switches first than the other because the dead time.

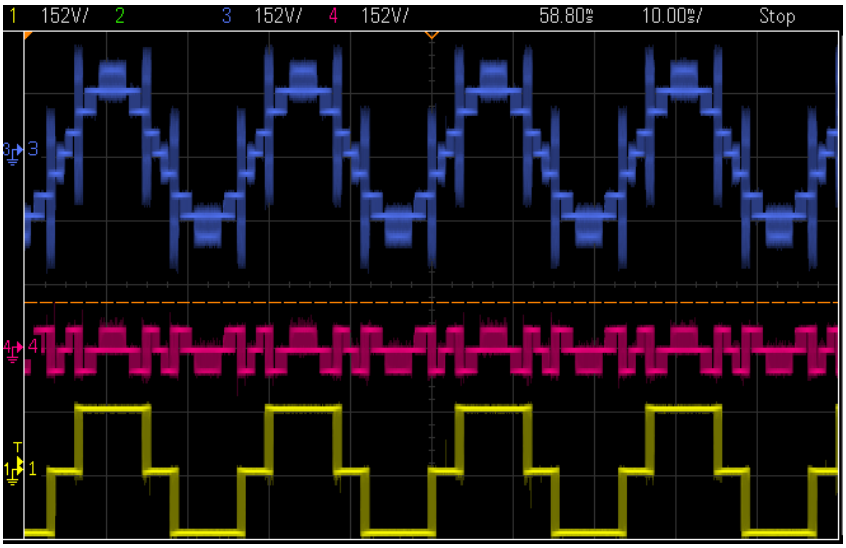

Figure 5-2 $V_{an}(t)$, $VH_l(t)$, $VHh(t)$

Figure 5-3 shows the output voltage $V_o(t)$(yellow), $V_{an}(t)$(blue), and $I_o(t)$(red). Notice that $V_o(t)$ has a small distortions in the intervals that $V_{an}(t)$ has the overshoots.

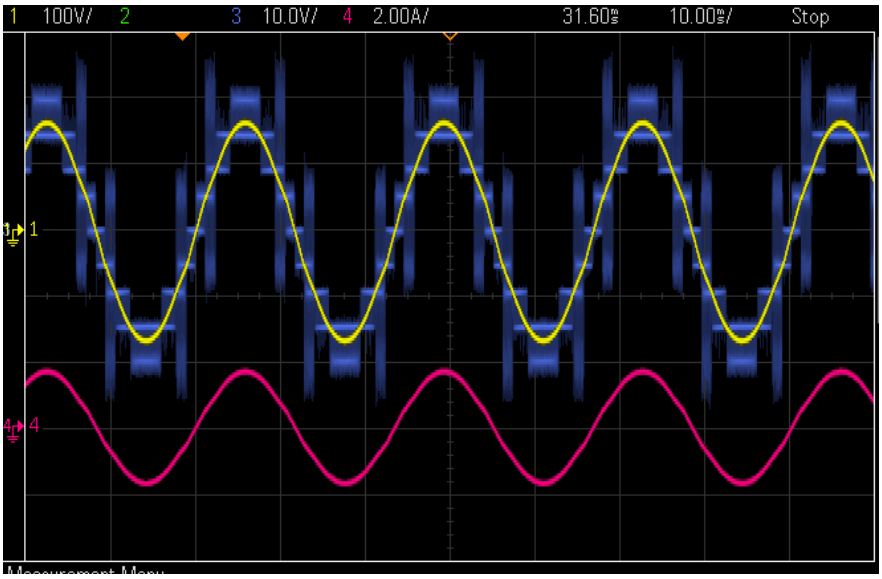

Figure 5-3 $V_o(t)$, $V_{an}(t)$, and $I_o(t)$.

The implementation in open loop with RC load was done to find the efficiency of the inverter, and determine how much power dissipates each element. Table 5.1 shows the power supplying of each H-Bridge($P_{150\ V}$,$P_{50\ V}$), the output Power (P_{out}), and the power losses of the output inductor, Higher H-Bridge and Lower H-Bridge.(P_{Lo}, P_{Lh}, P_{Ll}) and the respective percentage of the total power supplying.

P_x (power measures)	Power	Percentage (η)
P_{150V}	$215W$	100%
P_{out}	$200W$	93,03%
P_{50V}	$-2W$	0,93%
P_{L_o}	$0.3W$	0,14%
P_{L_h}	$1.5W$	0,7%
P_{L_l}	$0.18W$	0,08%

Table 5.1 Power in each part of the inverter.

Notice that the Source of 50 V, do not supply power, and consume a small quantity of power, this is because the source of 50 V serves to improve the THD not to supply power.

The losses in the switching devices are calculated with as:

$$P_{RDS} + P_{sw}$$

$$P_{150V} + P_{50V} = P_{out} + P_{L_o} + P_{L_h} + P_{L_l} + P_{RDS} + P_{sw} \quad \text{Eq. 5-1}$$

Where P_{RDS} are the conduction losses in the MOSFETs and P_{sw} the switching losses in the MOSFETs.

Accordingly the losses in the MOSFETs are:

$$P_{RDS} + P_{sw} = 11.02W$$

Figure 5-4 ripple current in open loop shows the ripple current in the inductor in open loop with RC load, and it is 300mA.

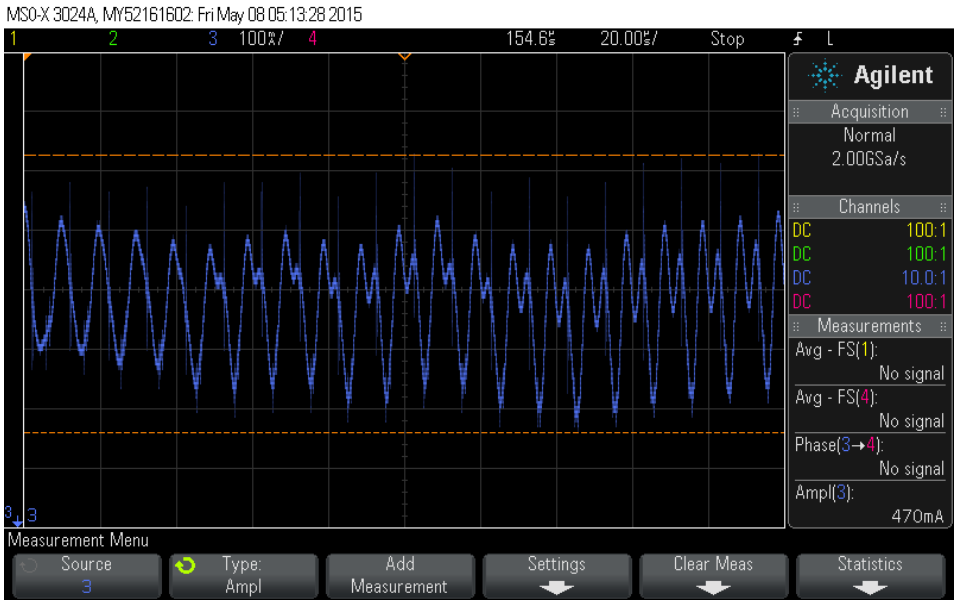

Figure 5-4 ripple current in open loop

5.2 Implementation of the linear control of the inverter in grid tie mode

In order that the controller will be implemented in a DSP the discrete controller has to be converted in a differences equation.

$$u(z) = e(z)G_{cd}(z)$$
$$u(z) = 0.9e(z)\frac{(1-0.99z^{-1})}{1-z^{-1}}$$
$$u_0 - u_{-1} = 0.9e_0 - 0.891e_{-1}$$

$$\boldsymbol{u_0 = u_{-1} + 0.9(e_0 - 0.99e_{-1})} \qquad \text{Eq. 5-2}$$

Eq. 5-2 shows the difference equation of the PI controller

Figure 5-5 linear controller with 1A peak in phaseshows the output current (red) and the grid voltage (yellow) with a current reference of 1A peak in phase. Notice the current ripple is approximately the 15% of the current amplitude.

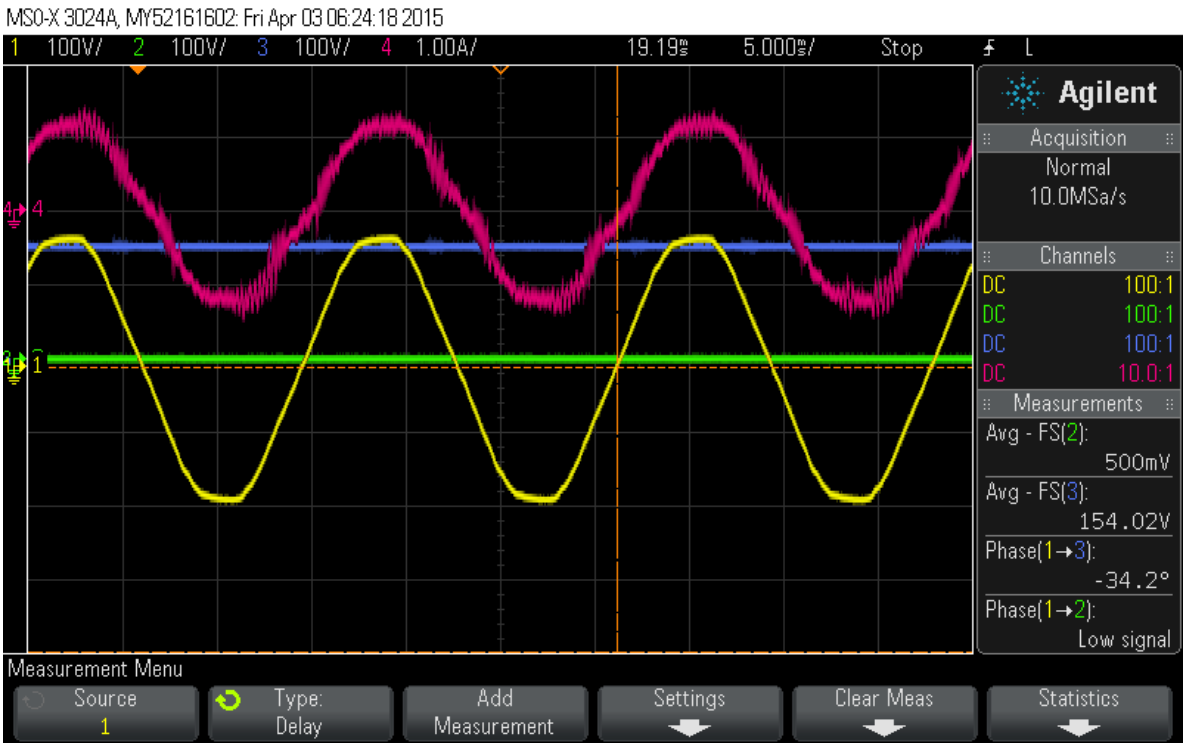

Figure 5-5 linear controller with 1A peak in phase

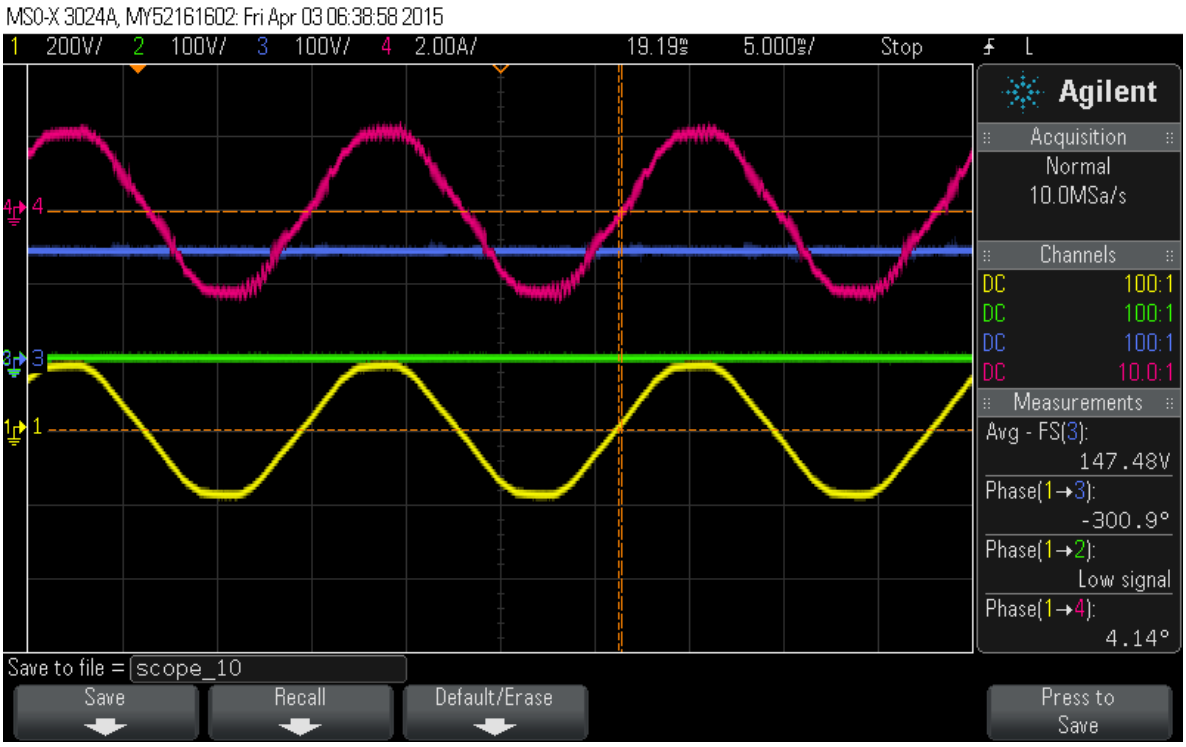

Figure 5-6 linear controller with 2A peak in phase

Figure 5-6 linear controller with 2A peak in phase shows the output current (red) and the grid voltage (yellow) with a current reference of 2A peak in phase. Notice the current ripple did not change if the amplitude reference is changed.

Figure 5-7 Linear controller with 1,7A peak in leading phaseshows the output current $i_o(t)$(blue) in phase leading, the grid voltage $v_{ac}(t)$ (green), and the total ouput voltages of the H-Bridges $v_{an}(t)$(yellow). Notice that the current is unstable in the intervals that $v_{an}(t)$ has the overshoots.

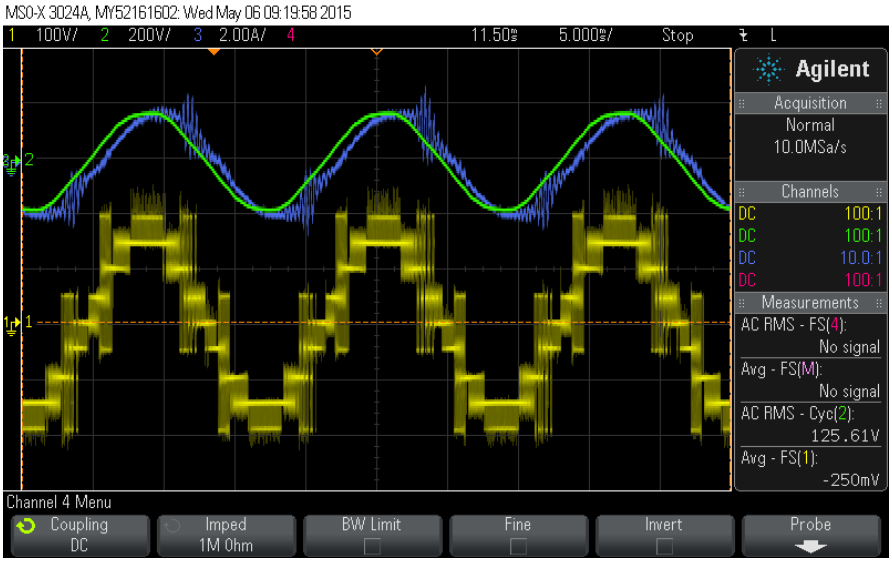

Figure 5-7 Linear controller with 1,7A peak in leading phase

Figure 5-8 shows the ripple current in the unstable zone and it is 1,5A. this ripple increase if the amplitude of $i_{ref}(t)$ increase.

Figure 5-8 ripple current in the unstable zone

Figure 5-9 shows the ripple current with linear controller in the stable zone, and it is 200mA. This ripple does not increase if the amplitude of I_{ref} increases.

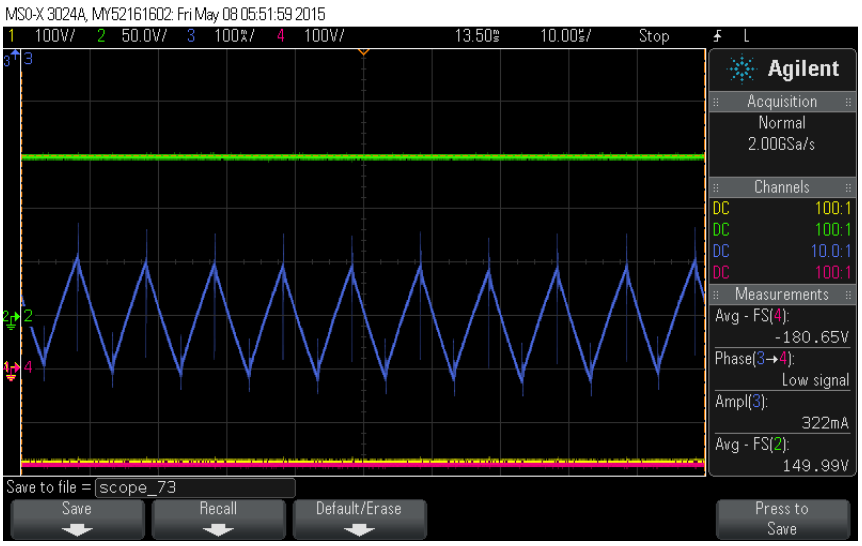

Figure 5-9 ripple current with linear controller in stable zone

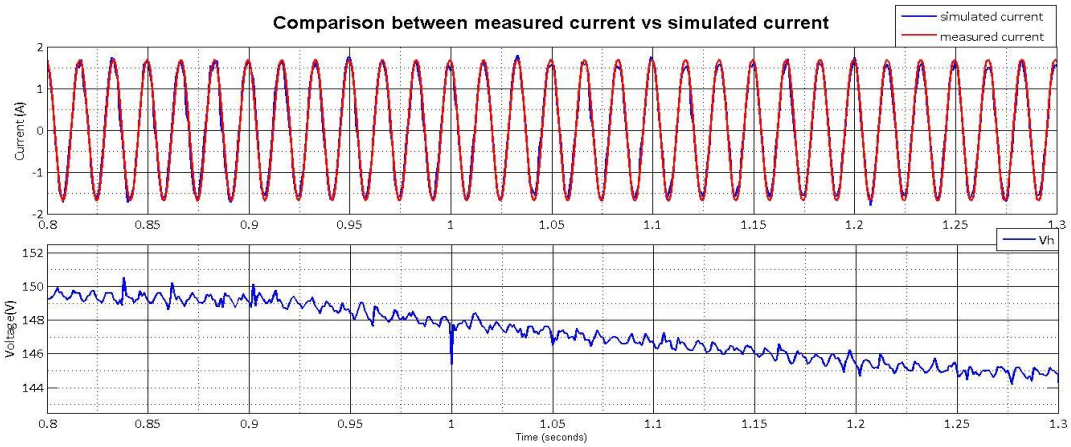

Figure 5-10 comparison between measured current vs simulated current changing Vh

Figure 5-10 shows a disturbance in the higher H-Bridge and the behavior of the simulated current and the measured current. Notice that those are very similar and the $e_{rms} = 0.27$ A

The e_{rms} between the reference and the measurement current in linear controller is 0,189 A.

5.3 Implementation of the sliding mode control.

In this chapter shows the results of the implementation of the nonlinear control

Figure 5-11shows the output current $i_o(t)$ (red) and the grid voltage (green) with a reference current of 1A peak in phase, notice the ripple current is almost the same as the linear controller.

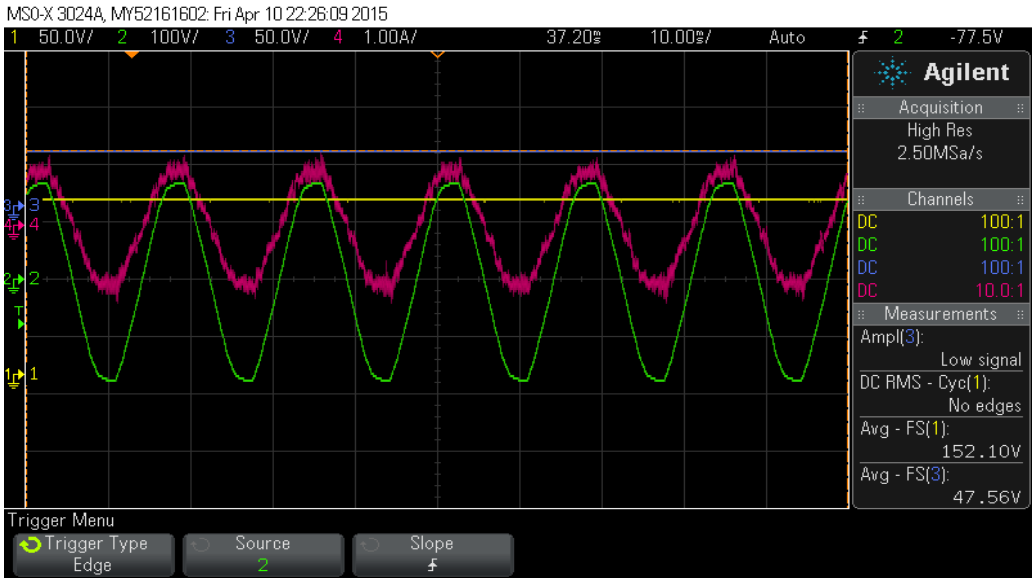

Figure 5-11 Io(t) with reference of 1A peak in phase

Figure 5-12 shows the output current $i_o(t)$ (red) and the grid voltage (blue) with a reference of 2A peak in phase, notice the ripple current is lower for the nonlinear controller.

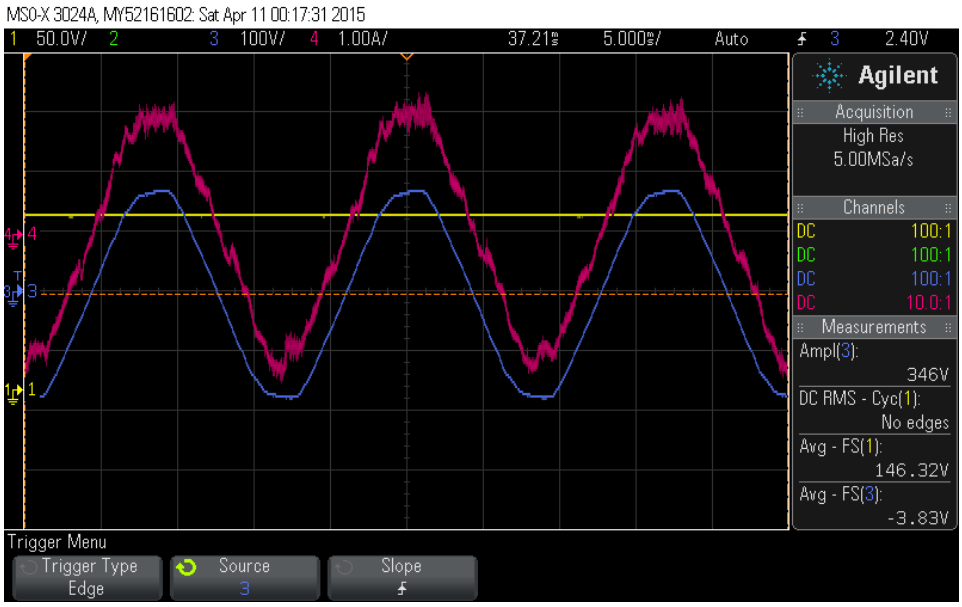

Figure 5-12 Io(t) with reference of 2A peak in phase

Figure 5-13 shows the output current $i_o(t)$ (red) and the grid voltage (blue and/or green) with a reference current of 2A peak and 43 degrees in lagging. Notice the nonlinear control the current ripple is less than the linear controller, and the current waveform is not distorted to phase change.

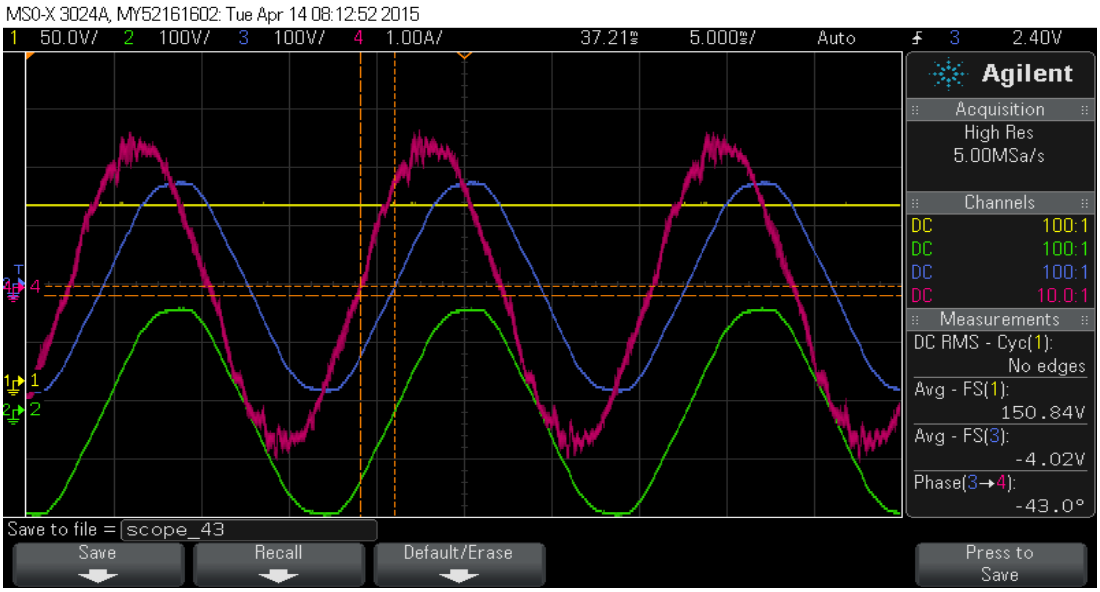

Figure 5-13 Io(t) with reference of 2A peak and 43 degrees in lagging

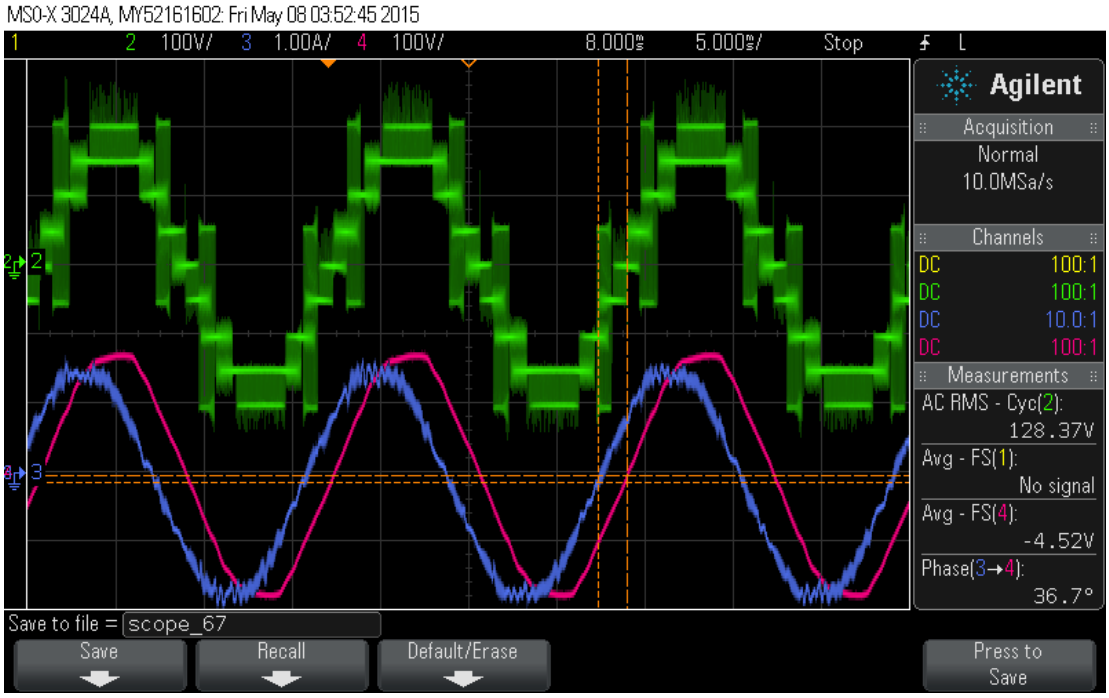

Figure 5-14 Van(t), Io(t) and Vac(t) with a reference of 1,5A peak and 36 degree in lagging.

Figure 5-14 shows the total output of the H-Bridges $v_{an}(t)$ (green) the output current $i_o(t)$(blue), and the grid voltage $v_{ac}(t)$ (red), when the reference is in lagging. Notice that the unstable zone in linear controller is stable in nonlinear controller.

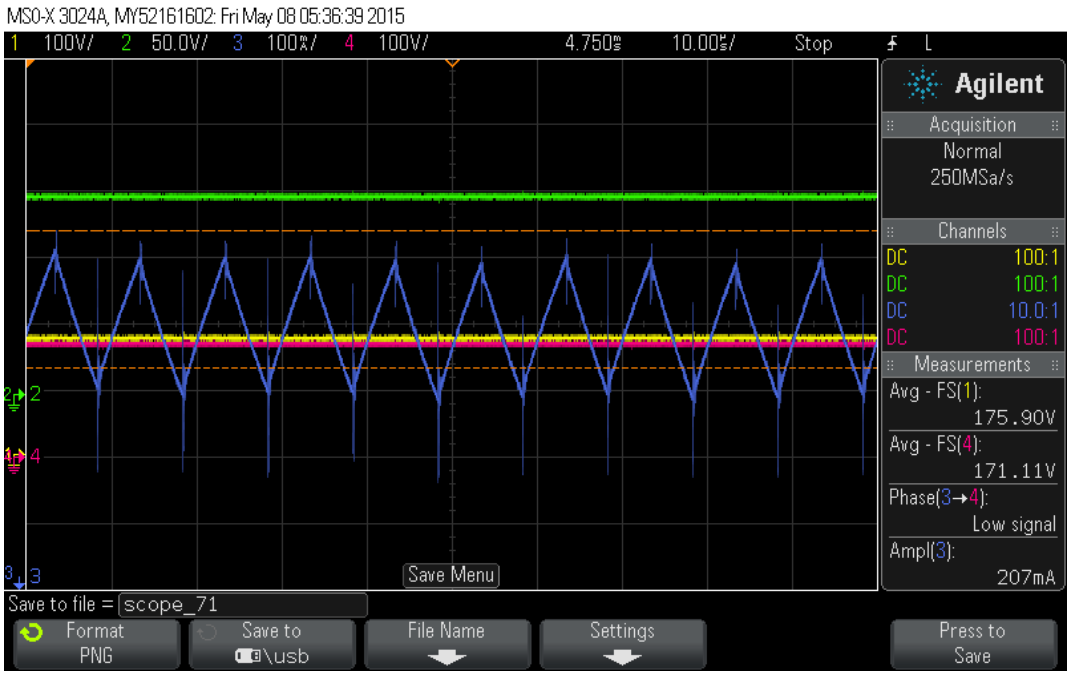

Figure 5-15 Ripple current with nonlinear controller

Figure 5-15 shows the ripple current with nonlinear controller, and it is 200mA. This ripple does not increase if amplitude of the current increase.

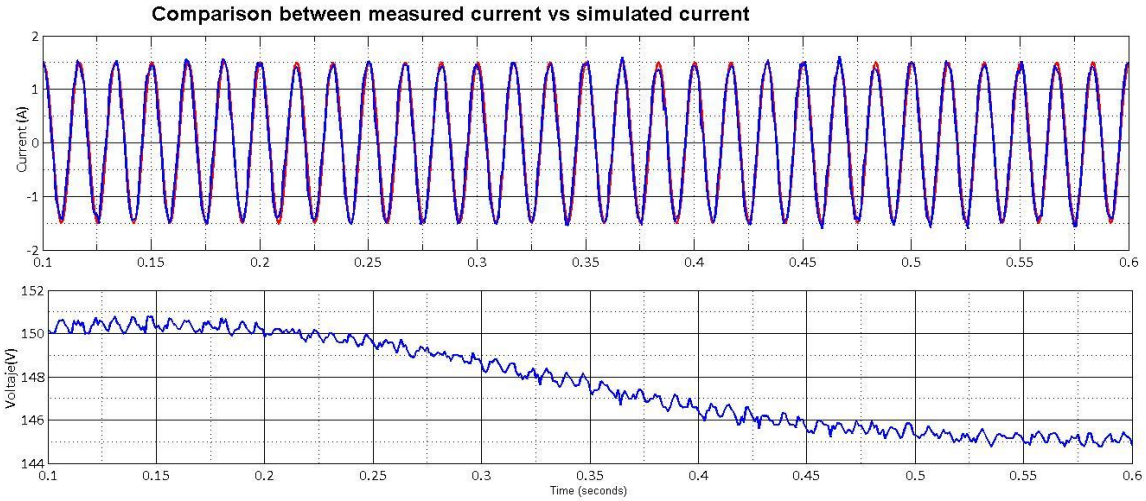

Figure 5-16 comparison between Io simulated and Io measured

Figure 5-16 comparison between Io simulated and Io measuredshows a disturbance in the higher H-Bridge and show the behavior of the simulated current and the measured current. Notice that are very similar and the $e_{rms} = 0.18$ A

The e_{rms}between the reference and the measurement current nonlinear controller is 0.06 A. The tracking error in nonlinear control is much lower than the linear controller.

6 Comparative analyses of results

The transient response time reference changes cannot be measure because the changes did softly

In the simulations the ripple current in the linear and nonlinear controller are the same of the open loop.

This probes were done with a variation of amplitude from 0,8A peak to 2,5 Apeak, and a variation of phase from -45 degrees to 45 degrees.

	Simulated			Measured		
	Open loop	**Linear controller**	**Nonlinear controller**	**Open Loop**	**Linear Controller**	**Nonlinear controller**
e_{rms}	-	99,8mA	18mA	-	190mA(Avg)	60mA (Avg)
e_{max}	-	270mA	100mA	-	-	-
Ripple current	100mA	100mA	100mA	300mA	1,5A	200mA
Transient response time reference change	-	80µs	450 µs	-	-	-

Table 6.1 Comparative analysis between simulated and measured circuits.

7 Conclusions:

- THMI is the inverter that has the most number of levels and this reduce the inductor dimension.
- Sub-harmonic PWM strategy is a straightforward modulation to implement in a THMI of 2 H-Bridges.
- To control a THMI a nonlinear control is better because it does not present problems with the intervals that may generate higher overshoots in the total outputs of the H-Bridges. The Sliding mode control defined in the project is a good control method because it ensures the stability independently of the value of the uncertainly while this do not tend to ∞.

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Appendix

In the DVDs attached to the document are the complementary files of this dissertation, which include each board schematic circuits, and the programs codes for the linear and nonlinear control in Code Composer Studio.